BT100A

HIGH-SPEED C²MOS INTEGRATED CIRCUITs

TC40H000 Series

Fist Edition·March. 1981

TOS

● HS-C²MOS FAMILY

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TC40H148P	16	8-LINE-TO-3-LINE PRIORITY ENCODER
TC40H151P	16	1-OF-8 DATA SELECTOR/MULTIPLEXER
TC40H160P	16	SYNCHRONOUS 4-BIT DECADE COUNTER
TC40H161P	16	SYNCHRONOUS 4-BIT BINARY COUNTER
TC40H162P	16	SYNCHRONOUS 4-BIT DECADE COUNTER
TC40H163P	16	SYNCHRONOUS 4-BIT BINARY COUNTER
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TC40H259P	16	8-BIT ADDRESSABLE LATCH
TC40H390P	16	DUAL DECADE COUNTER
TC40H393P	14	DUAL 4-BIT BINARY COUNTER

HS-C^{2}MOS IC

The surpassing features of CMOS are low power consumption, high noise immunity, wide range of operating voltage, large fan-out for CMOS to CMOS, and ability of high integration. On the other hand, however, its demerit is that the switching speed is lower than that of TTL.
To compensate this demerit, TOSHIBA has released a high speed CMOS under the name of HS-C^{2}MOS TC40H000P series since 1979.

In this new logic series, the conventional CMOS has been improved for the switching speed by the following methods;

(1) Improvement on process parameters
(2) Improvement on circuit construction
(3) Improvement on pattern layout

Through these improvements, the propagation delay time has been decreased to about 1/5 of the conventional time as shown in Fig. 1 and 2.

Fig. 3 shows a comparison among TTL, LS-TTL, conventional C^{2}MOS, and HS-C^{2}MOS on the maximum oscillating frequency of the ring oscillator in the gate IC. Also, it shows that HS-C^{2}MOS is approximately of the same as TTL in the characteristics of oscillator.

Fig. 4 shows a comparison between the input frequency vs. the current consumption in J-K flip-flop circuit. In case of the frequency under 10 - 20 MHz, HS-C^{2}MOS is smaller than LS-TTL in the power consumption. This is a major merit for operation.

Basically, HS-C^{2}MOS has the same designation as TTL or LS-TTL, in the lower three digits of the simbol by functions, and they have the lead-pins arranged in the same allocation.

Fig. 5 indicates a comparing list of various logic ICs in electrical characteristics.

On reliability including latch up, electrostatic durability, etc., it has been confirmed that HS-C^{2}MOS logic series can stand comparison with the conventional CMOS logic series.

Described in this technical data are the electrical characteristics of the high speed C^{2}MOS logic series containing the features mentioned above.

Fig. 1

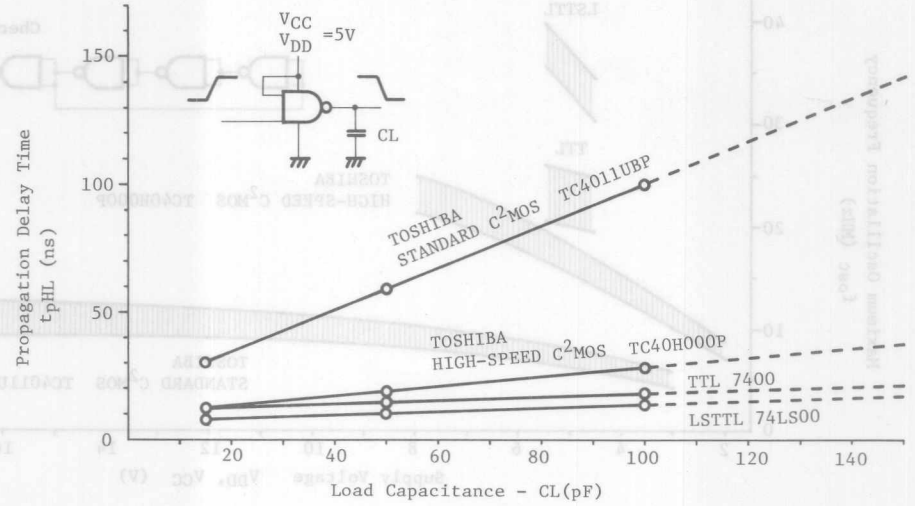

V_{CC}
V_{DD} =5V
CL
Propagation Delay Time
t_{pHL} (ns)
150
100
50
0
TOSHIBA
STANDARD C^2MOS TC4011UBP
TOSHIBA
HIGH-SPEED C^2MOS TC40H000P
TTL 7400
LSTTL 74LS00
20
40
60
80
100
120
140
Load Capacitance - CL(pF)

Fig. 2

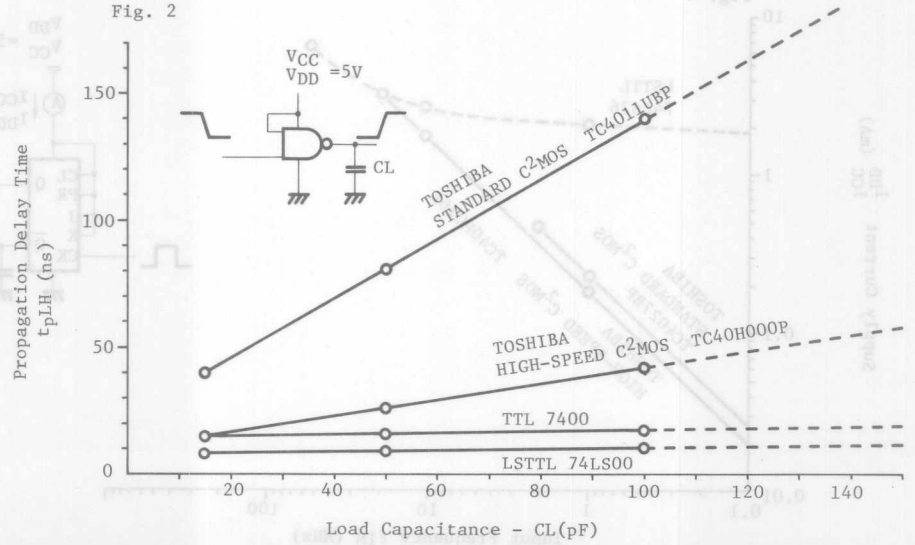

V_{CC}
V_{DD} =5V
CL
Propagation Delay Time
t_{pLH} (ns)
150
100
50
0
TOSHIBA
STANDARD C^2MOS TC4011UBP
TOSHIBA
HIGH-SPEED C^2MOS TC40H000P
TTL 7400
LSTTL 74LS00
20
40
60
80
100
120
140
Load Capacitance - CL(pF)

Fig. 3

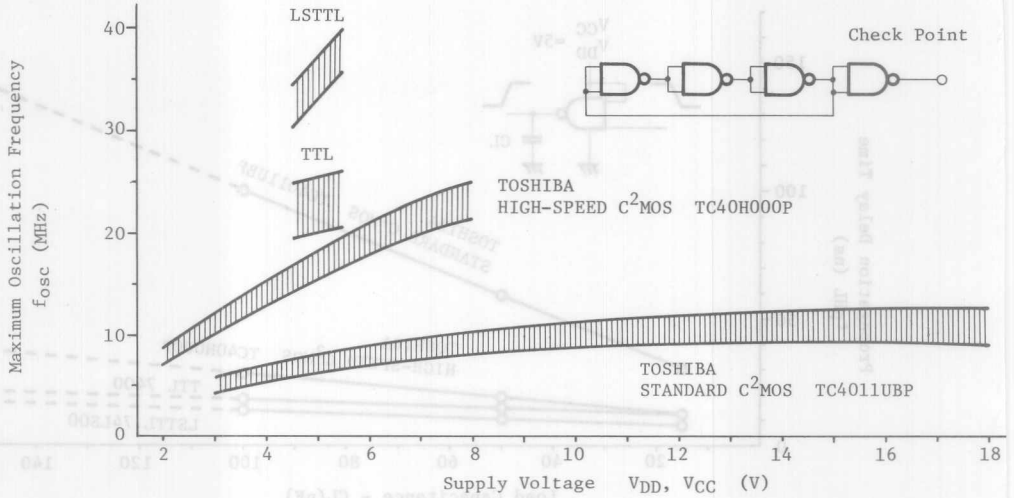

LSTTL
TTL
Check Point
TOSHIBA
HIGH-SPEED C2MOS TC40H000P
TOSHIBA
STANDARD C2MOS TC4011UBP
Maximum Oscillation Frequency
fosc (MHz)
Supply Voltage VDD, VCC (V)
0
10
20
30
40
2
4
6
8
10
12
14
16
18

Fig. 4

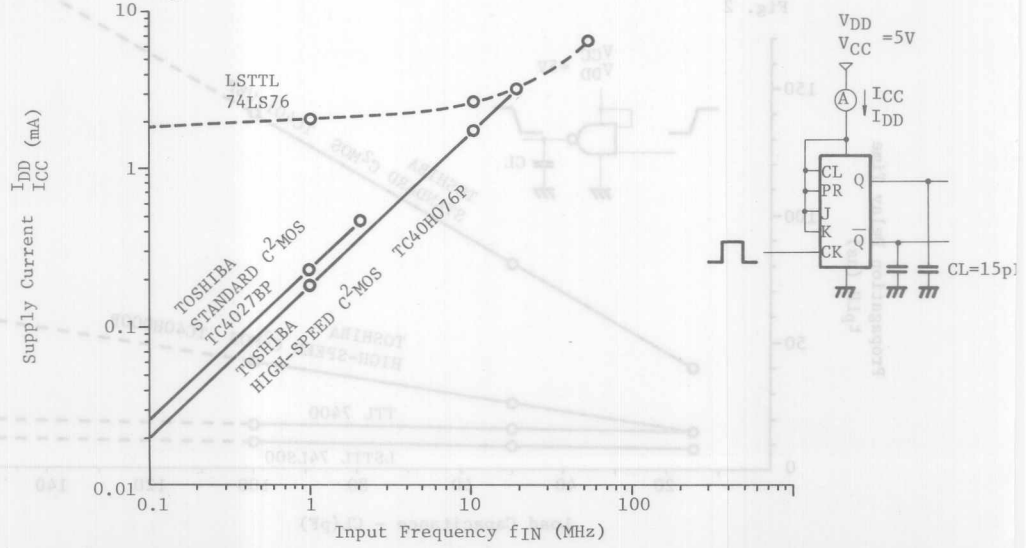
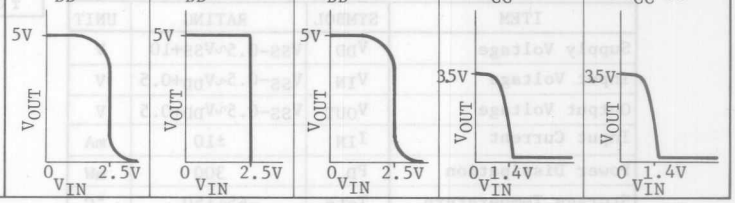

LSTTL
74LS76
TOSHIBA
STANDARD C2MOS
TC4027BP
TOSHIBA
HIGH-SPEED C2MOS TC40H076P
Supply Current IDD ICC (mA)
Input Frequency fIN (MHz)
0.01
0.1
1
10
100
VDD
VCC =5V
A
ICC
IDD
CL
PR
J
K
CK
Q
CL=15pF

Fig. 5

Comparison of Logic IC (2-Input NAND GATE)

Parameter	HS-C²MOS	B-type CMOS	UB-type CMOS	TTL	LSTTL
DC Supply Voltage	2 ∿ 8V	3 ∿ 18V	3 ∿ 18V	5 ± 5% V	5 ± 5% V
Operating Temperature	-40 ∿ 85°C	-40 ∿ 85°C	-40 ∿ 85°C	0 ∿ 70°C	0 ∿ 70°C
Switching Time	15 ns	125 ns	60 ∿ 100 (ns)	10 ns	5 ns
Low Level Output Current $V_{DD}=V_{CC}=5V$	0.8 mA	0.44 mA	0.44 mA	16 mA	8 mA
Power Dissipation/ $V_{DD}=V_{CC}=5V$ Gate	1.0 mW (f_{IN}=1MHz)	1.0 mW (f_{IN}=1MHz)	1.0 mW (f_{IN}=1MHz)	10 mW	2 mW
Noise	Good!	Excellent!!	Excellent!!	Poor	Poor
Latch up	Yes	Yes	Yes	No	No
V_{IN}-V_{OUT} Characteristics (Ta=25°C)	V_{DD}=5V	V_{DD}=5V	V_{DD}=5V	V_{CC}=5V	V_{CC}=5V

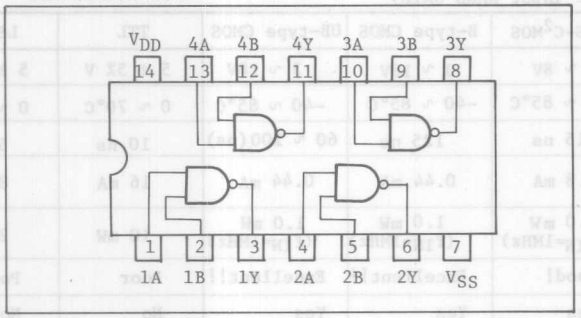


"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H000P
SILICON MONOLITHIC

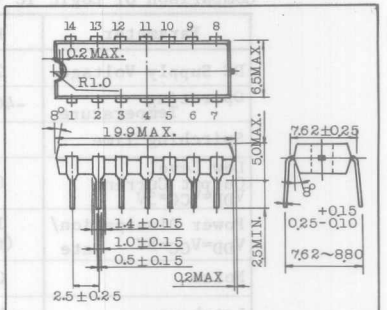
TENTATIVE

TC40H000P QUAD 2-INPUT NAND GATES

PIN CONNECTION



Unit in mm



JEDEC	—
TOSHIBA	5-21F

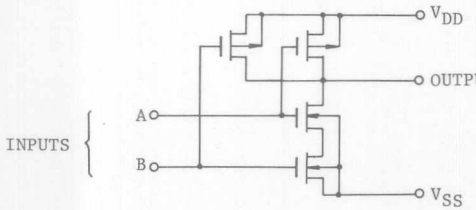
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	Tstg	-65∿150	°C
Lead Temperature/Time	Tsol	260°C·10sec	

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

CIRCUIT DIAGRAM



* With all inputs and protection circuit contained.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{DD}$	5	-	0.05	-	0.0	0.05		0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{DD}$	5	1.4	-	1.1		-	0.8	-	mA
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\|$ <1μA V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
	Low Level	V_{IL}	V_{OUT}=4.5V	5	-	10	-		1.0	-	1.0	V
Input Current	High Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	Low Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig. 1	5	-	28	40	ns
Output Fall Time		t_{of}	Fig. 1	5	-	16	30	ns
Propagation Delay Time	Low-High	t_{PLH}	Fig. 1	5	-	19	26	ns
	High-Low	t_{PHL}		5	-	14	21	ns
Propagation Delay Time	Low-High	t_{PLH}	Fig. 2	5	-	13	20	ns
	High-Low	t_{PHL}		5	-	15	23	ns
Input Capacitance		C_{IN}			-	5	-	pF

SWITCHING TIME TEST CIRCUITS

Fig. 1

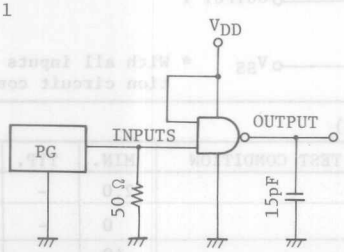
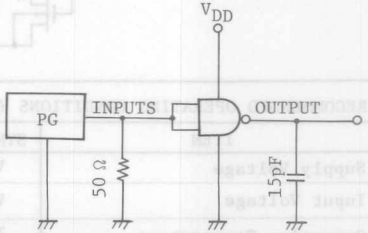


Fig. 2



Toshiba **INTEGRATED CIRCUIT**

TECHNICAL DATA

"C²MOS" DIGITAL INTEGRATED CIRCUIT

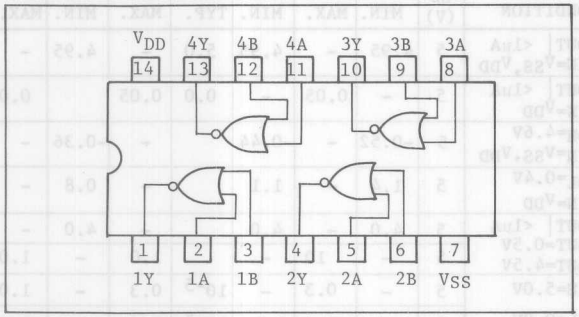
TC40H002P

SILICON MONOLITHIC

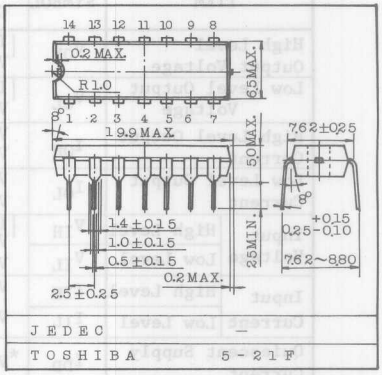
TENTATIVE

TC40H002P QUAD 2-INPUT NOR GATES

PIN CONNECTION



Unit in mm



JEDEC —

TOSHIBA 5-21F

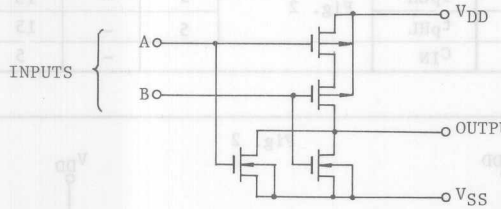
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storag Temperature	T_{stg}	-65∿150	°C
Lead Temperature/ Time	T_{sol}	260°C·10sec	

TRUTH TABLE

INPUTS A	INPUTS B	OUTPUT Y
L	L	H
L	H	L
H	L	L
H	H	L

CIRCUIT DIAGRAM



* With all inputs and protection circuit contained.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

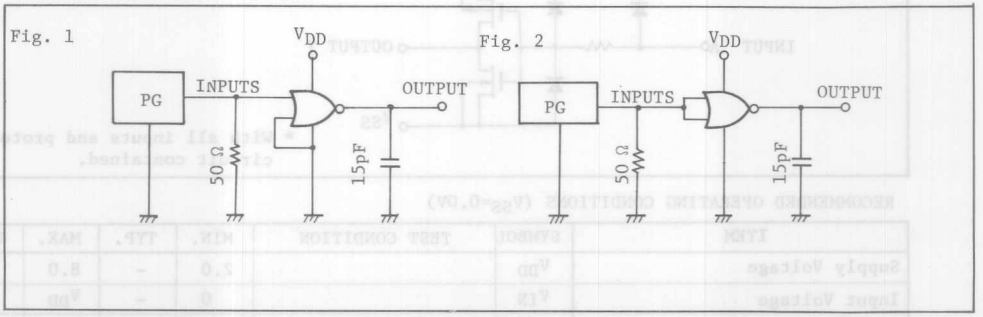
ITEM		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05		0.05	
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1		-	0.8	-	
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\|$ <1μA	5	4.0	-	4.0		-	4.0	-	V
	Low Level	V_{IL}	V_{OUT}=0.5V V_{OUT}=4.5V	5	-	1.0	-		1.0	-	1.0	
Input Current	High Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	Low Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.-	
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	-10^{-3}	2.0	-	10.0	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig. 1	5	-	23	37	ns
Output Fall Time		t_{of}	Fig. 1	5	-	17	37	
Propagation Delay Time	Low-High	t_{pLH}	Fig. 1	5	-	18	27	ns
	High-Low	t_{pHL}		5	-	17	25	
Propagation Delay Time	Low-High	t_{pLH}	Fig. 2	5	-	18	27	
	High-Low	t_{pHL}		5	-	13	20	
Input Capacitance		C_{IN}			-	5	-	pF

SWITCHING TIME TEST CIRCUITS



Toshiba **INTEGRATED CIRCUIT**

TECHNICAL DATA

"C^2MOS" DIGITAL INTEGRATED CIRCUIT

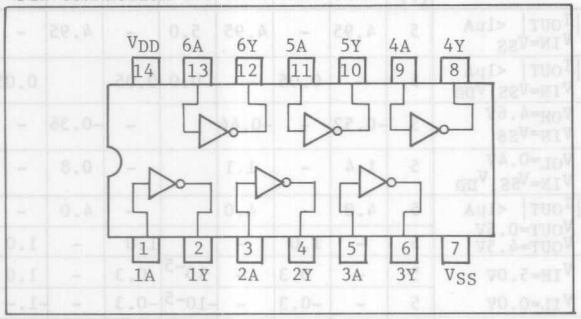
TC40H004P

SILICON MONOLITHIC

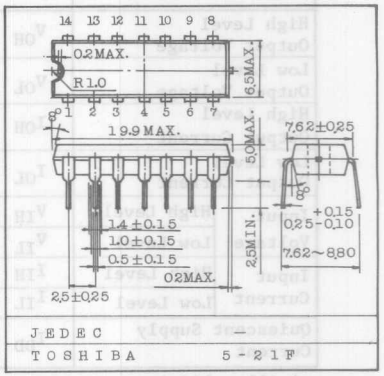
TENTATIVE

TC40H004P HEX INVERTERS

PIN CONNECTION



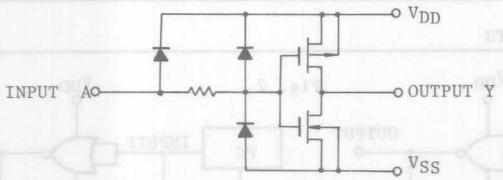
Unit in mm



MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature/ Time	T_{sol}	260°C·10sec	

CIRCUIT DIAGRAM



* With all inputs and protection circuit contained.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{DD}$	5	1.4	-	1.1		-	0.8	-	mA
High Level Input Voltage		V_{IH}	$\|I_{OUT}\|$<1μA V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
Low Level Input Voltage		V_{IL}	V_{OUT}=4.5V $V_{IN}=V_{SS}, V_{DD}$	5	-	1.0	-		1.0	-	1.0	V
Input Current	High Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	Low Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS}, V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

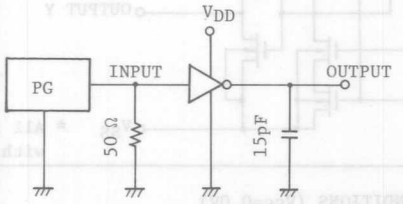
*All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig. 1	5	-	14	30	ns
Output Fall Time		t_{of}	Fig. 1	5	-	11	30	ns
Propagation Delay Time	Low-High	t_{pLH}	Fig. 1	5	-	15	20	ns
	High-Low	t_{pHL}		5	-	13	20	ns
Input Capacitance		C_{IN}			-	5	-	pF

SWITCHING TIME TEST CIRCUITS

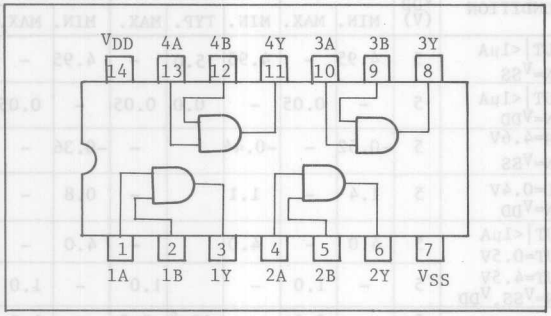
Fig. 1



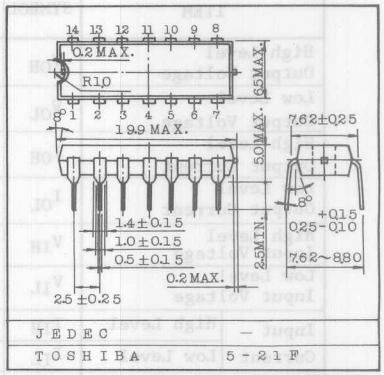
"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H008P
SILICON MONOLITHIC

TENTATIVE
EC40H008P TRIPLE 3-INPUT AND GATES

PIN CONNECTION



Unit in mm



JEDEC —
TOSHIBA 5-21F

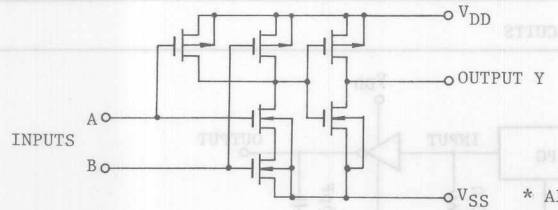
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{SS}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{SS}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temp./Time	T_{sol}	260°C·10sec	

TRUTH TABLE

INPUTS		OUTPUT
B	A	Y
L	L	L
L	H	L
H	L	L
H	H	H

CIRCUIT DIAGRAM



* All inputs are equipped with protection circuit.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-4.0	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS}, V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{DD}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS}, V_{DD}$	5	1.4	-	1.1		-	0.8	-	
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\|$<1μA V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
	Low Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-		1.0	-	1.0	
Input Current	"L" Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"H" Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Current Consumption		I_{DD}	*$V_{IN}=V_{SS}, V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig. 1	5	-	20	33	ns
Output Fall Time		t_{of}	Fig. 1	5	-	14	26	
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 1	5	-	15	23	ns
	(H-L)	t_{pHL}		5	-	19	26	
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 2	5	-	16	23	
	(H-L)	t_{pHL}		5	-	14	21	
Input Capacitance		C_{IN}			-	5	-	pF

SWITCHING TIME TEST CIRCUITS

Fig. 1

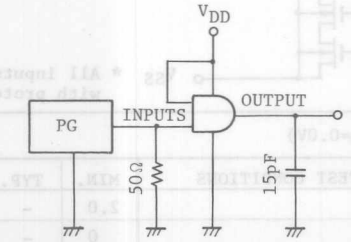
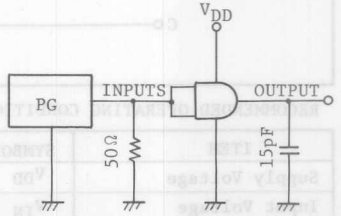


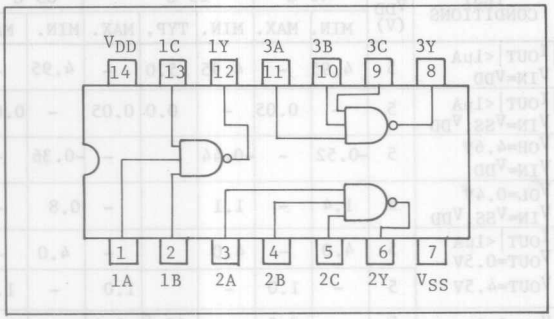
Fig. 2



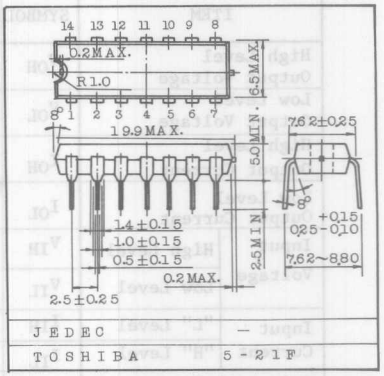
"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H010P
SILICON MONOLITHIC

TENTATIVE
TC40H010P TRIPLE 3-INPUT NAND GATES

PIN CONNECTION



Unit in mm



JEDEC	—
TOSHIBA	5-21F

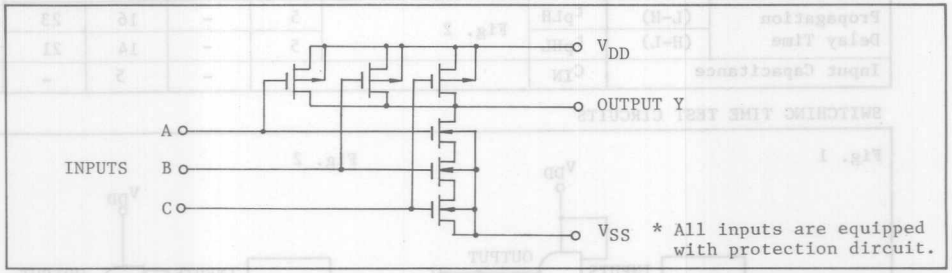
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	Tstg	-65∿150	°C
Lead Temp./Time	T_{sol}	260°C·10sec	

TRUTH TABLE

INPUTS			OUTPUT
C	B	A	Y
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

CIRCUIT DIAGRAM



* All inputs are equipped with protection dircuit.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{DD}$	5	1.4	-	1.1		-	0.8	-	mA
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\|$ <1μA V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
	Low Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-		0.3	-	1.0	V
Input Current	"H" Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig. 1	5	-	25	50	ns
Output Fall Time		t_{of}	Fig. 1	5	-	17	40	ns
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 1	5	-	25	50	ns
	(H-L)	t_{pHL}		5	-	18	40	ns
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 2	5	-	14	30	ns
	(H-L)	t_{pHL}		5	-	20	40	ns
Input Capacitance		C_{IN}			-	5		pF

SWITCHING TIME TEST CIRCUITS

Fig. 1

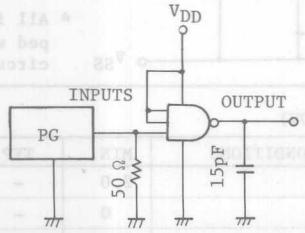
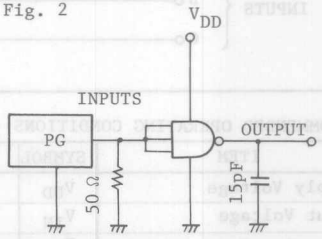


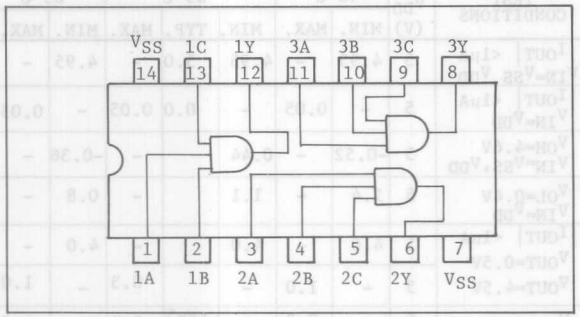
Fig. 2

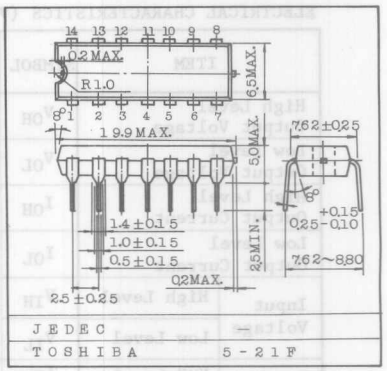


"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H011P
SILICON MONOLITHIC

Unit in mm

TENTATIVE
TC40H011P TRIPLE 3-INPUT AND GATES
PIN CONNECTION





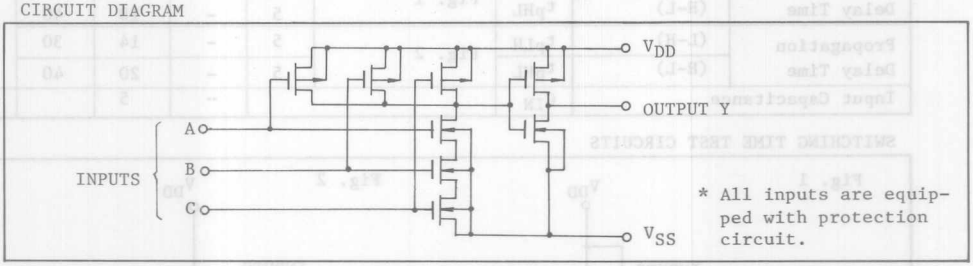
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temp./Time	T_{sol}	260°C·10sec	

TRUTH TABLE

INPUT			OUTPUT
C	B	A	Y
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

CIRCUIT DIAGRAM



* All inputs are equipped with protection circuit.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{DD},V_{SS}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{DD}$	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{DD},V_{SS}$	5	1.4	-	1.1	-	-	0.8	-	mA
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\|$ <1μA V_{OUT}=0.5V	5	4.0	-	4.0	-		4.0		V
	Low Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-	-	1.0	-	1.0	V
Input Current	"H" Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Current Consumption		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig. 1	5	-	20	40	ns
Output Fall Time		t_{of}	Fig. 1	5	-	18	40	ns
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 1	5	-	25	50	ns
	(H-L)	t_{pHL}		5	-	30	60	ns
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 2	5	-	30	60	ns
	(H-L)	t_{pHL}		5	-	25	50	ns
Input Capacitance		C_{IN}			-	5		pF

SWITCHING TIME TEST CIRCUITS

Fig. 1

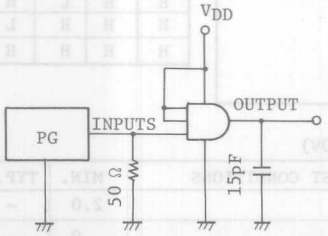
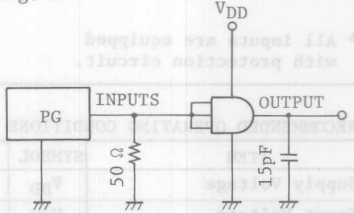


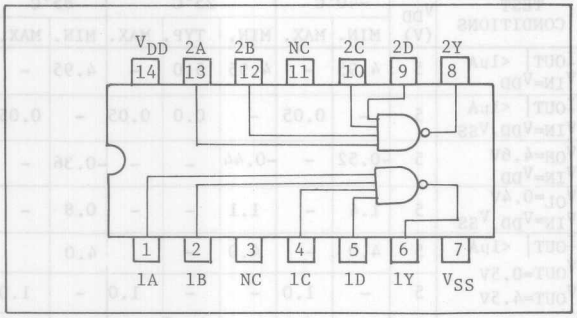
Fig. 2



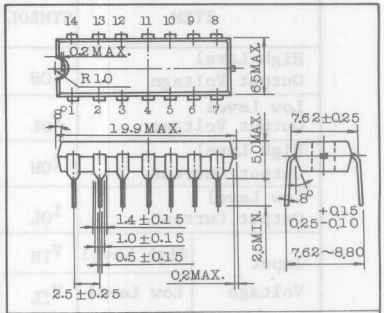
"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H020P
SILICON MONOLITHIC

TENTATIVE
TC40H020P DUAL 4-INPUT NAND GATES

PIN CONNECTION



Unit in mm

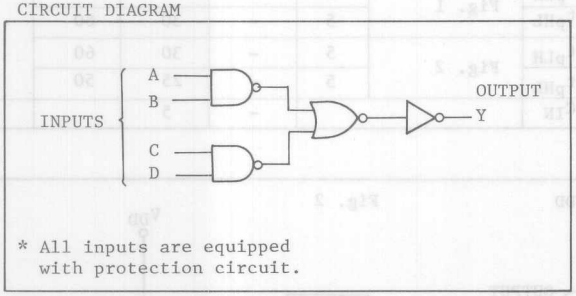


JEDEC	—
TOSHIBA	5-21F

MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{SS}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	Tstg	-65~150	°C
Lead Temp./Time	Tsol	260°C·10 sec	

CIRCUIT DIAGRAM



* All inputs are equipped with protection circuit.

TRUTH TABLE

INPUTS				OUTPUT
D	C	B	A	Y
L	L	L	L	H
L	L	L	H	H
L	L	H	L	H
L	L	H	H	H
L	H	L	L	H
L	H	L	H	H
L	H	H	L	H
L	H	H	H	H
H	L	L	L	H
H	L	L	H	H
H	L	H	L	H
H	L	H	H	H
H	H	L	L	H
H	H	L	H	H
H	H	H	L	H
H	H	H	H	L

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{DD}$	5	-	0.05	-	0.0	0.05		0.05	V
High Level Output Current		I_{OH}	I_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{DD}$	5	1.4	-	1.1		-	0.8	-	mA
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\|$ <1μA V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
	Low Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-		1.0	-	1.0	V
Input Current	"H" Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Current Consumption		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig. 1	5	-	20	40	ns
Output Fall Time		t_{of}	Fig. 1	5	-	20	40	ns
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 1	5	-	30	60	ns
	(H-L)	t_{pHL}		5	-	25	50	ns
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 2	5	-	20	40	ns
	(H-L)	t_{pHL}		5	-	25	50	ns
Input Capacitance		C_{IN}			-	5	-	pF

SWITCHING TIME TEST CIRCUITS

Fig. 1

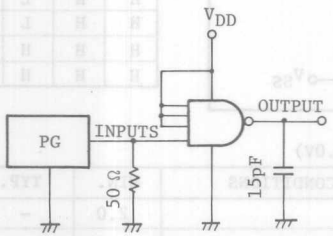
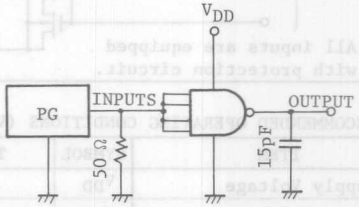


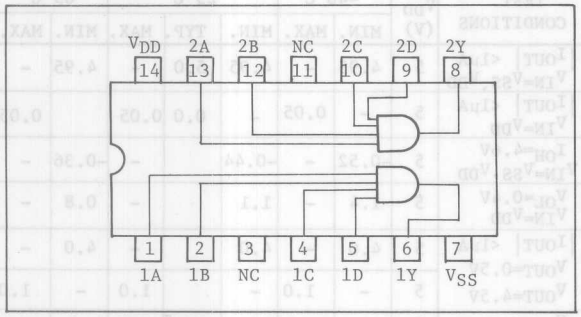
Fig. 2



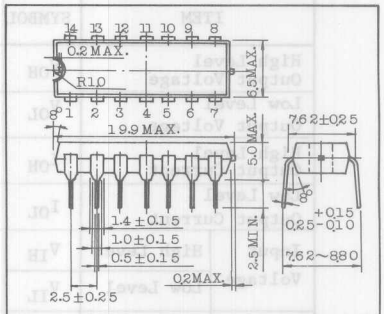
"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H021P
SILICON MONOLITHIC

TENTATIVE
TC40H021P DUAL 4-INPUT AND GATES

PIN CONNECTION



Unit in mm



JEDEC	—
TOSHIBA	5-21F

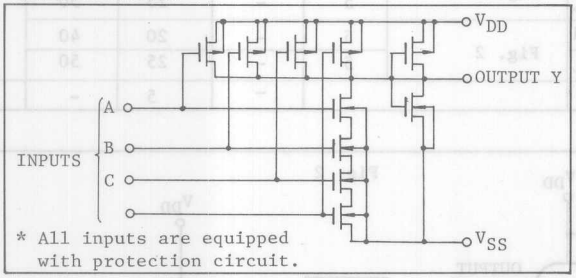
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temp./Time	T_{sol}	260°C·10 sec	

TRUTH TABLE

INPUTS				OUTPUT
D	C	B	A	Y
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	L
L	H	L	L	L
L	H	L	H	L
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
H	L	L	H	L
H	L	H	L	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	H

CIRCUIT DIAGRAM



* All inputs are equipped with protection circuit.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C		25°C		85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS}, V_{DD}$	5	-	0.05	-	0.0	0.05		0.05	
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{DD}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS}, V_{DD}$	5	1.4	-	1.1		-	0.8	-	
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\|$ <1μA V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
	Low Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-		1.0	-	1.0	
Input Current	"H" Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS}, V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig. 1	5	-	20	40	ns
Output Fall Time		t_{of}	Fig. 1	5	-	20	40	
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 1	5	-	23	50	ns
	(H-L)	t_{pHL}		5	-	25	50	
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 2	5	-	20	40	
	(H-L)	t_{pHL}		5	-	20	40	
Input Capacitance		C_{IN}			-	5	-	pF

SWITCHING TIME TEST CIRCUITS

Fig. 1

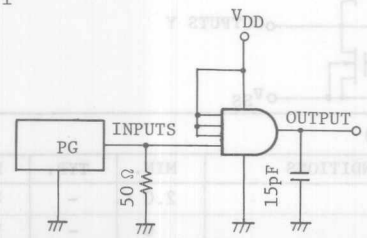
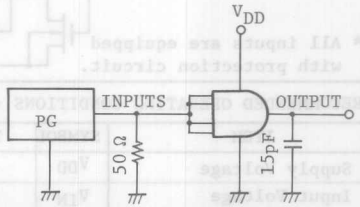


Fig. 2



Toshiba **INTEGRATED CIRCUIT**

TECHNICAL DATA

"C²MOS" DIGITAL INTEGRATED CIRCUIT

TC40H027P

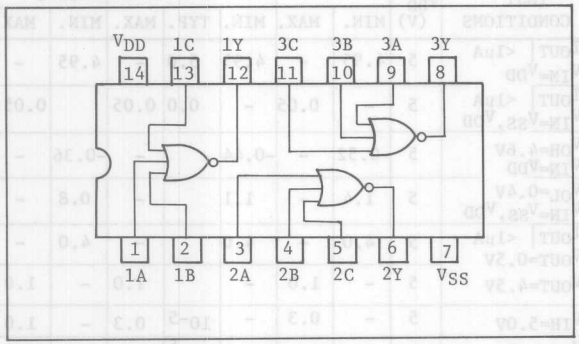
SILICON MONOLITHIC

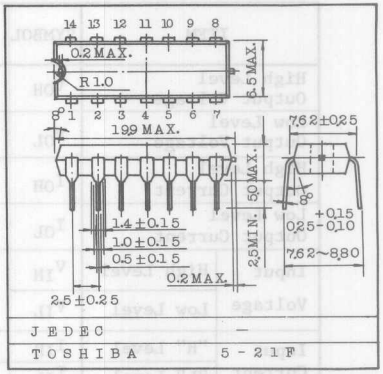
TENTATIVE

Unit in mm

TC40H027P TRIPLE 3-INPUT NOR GATES

PIN CONNECTION





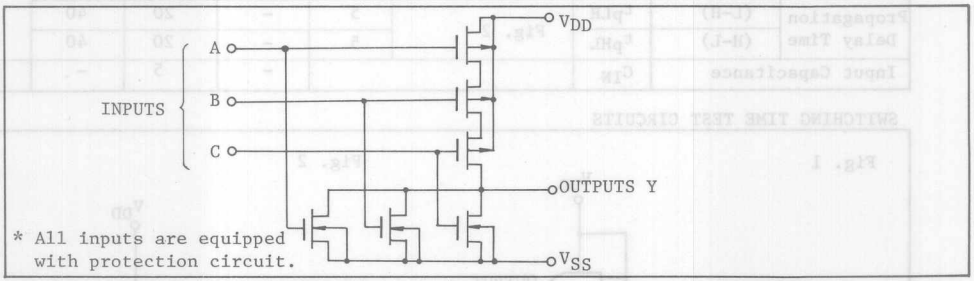
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temp.	T_{stg}	-65~150	°C
Lead Temp./Time	T_{sol}	260°C·10 sec	

TRUTH TABLE

INPUTS			OUTPUT
A	B	C	
L	L	L	H
H	L	L	L
L	H	L	L
H	H	L	L
L	L	H	L
H	L	H	L
L	H	H	L
H	H	H	L

CIRCUITS DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1		-	0.8	-	
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\|$ <1μA V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
	Low Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-		1.0	-	1.0	
Input Current	"H" Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig. 1	5	-	20	40	ns
Output Fall Time		t_{of}	Fig. 1	5	-	20	40	
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 1	5	-	20	40	ns
	(H-L)	t_{pHL}		5	-	23	50	
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 2	5	-	20	40	
	(H-L)	t_{pHL}		5	-	15	30	
Input Capacitance		C_{IN}			-	5	-	pF

SWITCHING TIME TEST CIRCUITS

Fig. 1

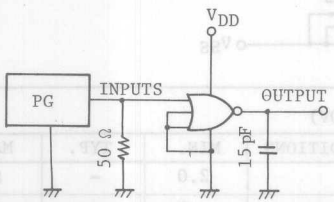
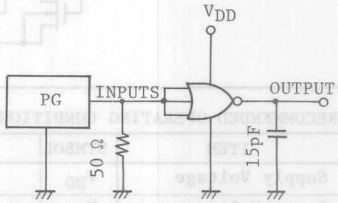


Fig. 2

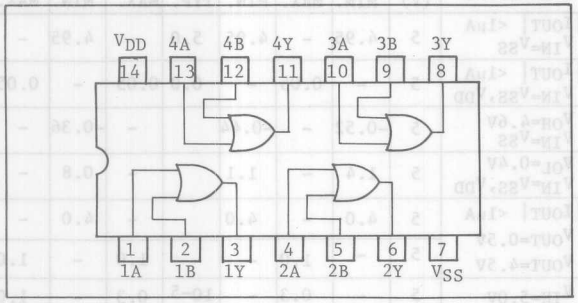


"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H032P
SILICON MONOLITHIC

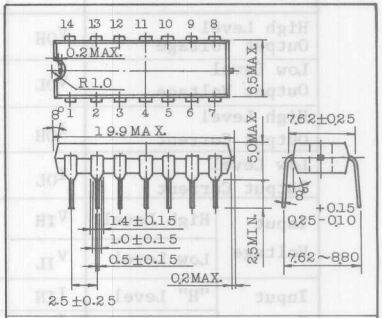
TENTATIVE

TC40H032P QUAD 2-INPUT OR GATES

PIN CONNECTION



Unit in mm



JEDEC	—
TOSHIBA	5-21F

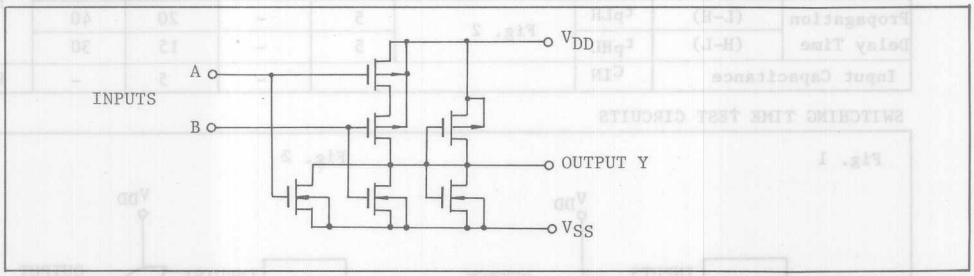
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temp./Time	T_{sol}	260°C·10 sec	

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

CIRCUIT DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temp.	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS}$	5	1.4	-	1.1		-	0.8	-	mA
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\|$ <1μA V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
	Low Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-		1.0	-	1.0	V
Input Current	"H" Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig. 1	5	-	20	40	ns
Output Fall Time		t_{of}	Fig. 1	5	-	20	40	ns
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 1	5	-	25	50	ns
	(H-L)	t_{pHL}		5	-	20	40	ns
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 2	5	-	20	40	ns
	(H-L)	t_{pHL}		5	-	23	50	ns
Input Capacitance		C_{IN}			-	5	-	pF

SWITCHING TIME TEST CIRCUITS

Fig. 1

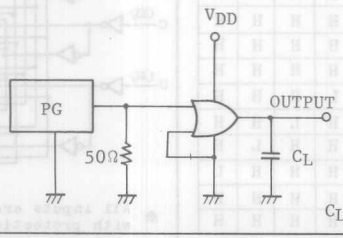
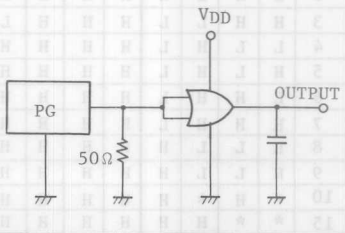


Fig. 2



"C²MOS" DIGITAL INTEGRATED CIRCUIT

TC40H042P

SILICON MONOLITHIC

TC40H042P BCD-TO-DECIMAL DECODER/DRIVER

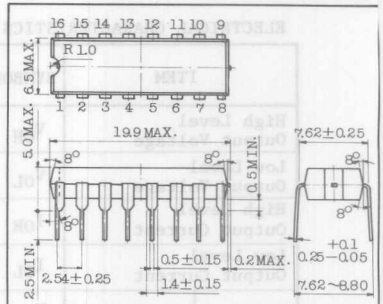
Unit in mm

TC40H042P is a BCD-TO-DECIMAL DECODER that converts BCD signal into the decimal signal.

The output which corresponds to BCD input code becomes "L" level, and all the other outputs become "H" level.

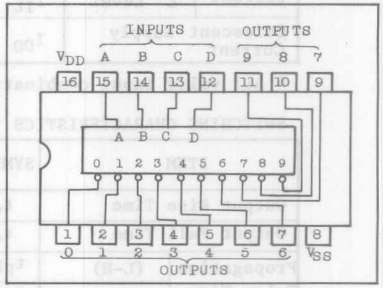
Also, all the outputs of more than BCD input code "10" become "H" level.

The functions and pin assignments of TC40H042P are the same as those of 74LS42.



JEDEC	—
TOSHIBA	5-22E

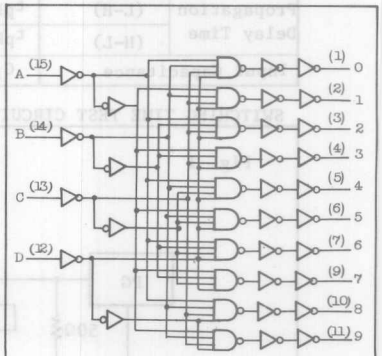
PIN CONNECTION



MASIMUM RATINGS

ITEM	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature/Time	T_{sol}	260°C · 10 sec	

LOGIC DIAGRAM



※ All inputs are equipped with protection circuit.

TRUTH TABLE

No.	BCD INPUTS				DECIMAL OUTPUTS									
	A	B	C	D	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	H	L	L	L	H	L	H	H	H	H	H	H	H	H
2	L	H	L	L	H	H	L	H	H	H	H	H	H	H
3	H	H	L	L	H	H	H	L	H	H	H	H	H	H
4	L	L	H	L	H	H	H	H	L	H	H	H	H	H
5	H	L	H	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	H	H	H	L	H	H	H	H	H	H	H	L	H	H
8	L	L	L	H	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	*	H	*	H	H	H	H	H	H	H	H	H	H	H
15	*	*	H	H	H	H	H	H	H	H	H	H	H	H

* = Don't care

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05		0.05	
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-1.04	-	-0.88		-	-0.72	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	2.8	-	2.2		-	1.6	-	
Input Voltage	"H" Level	V_{IH}	$\|I_{OUT}\|$<1μA V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
	"L" Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-		1.0	-	1.0	
Input Current	"H" Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=50 pF)

ITEM		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}			20	35	ns
Output Fall Time		t_{of}			16	29	
Propagation Delay Time	"L" to "H" Level	t_{pLH}			36	50	ns
	"H" to "L" Level	t_{pHL}			33	46	

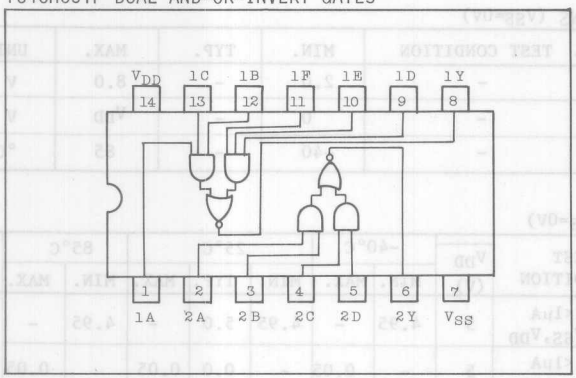
"C²MOS" DIGITAL INTEGRATED CIRCUIT

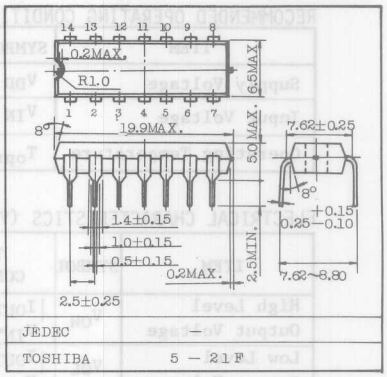
TC40H051P

SILICON MONOLITHIC

TC40H051P DUAL AND-OR-INVERT GATES

Unit in mm





JEDEC	—
TOSHIBA	5 − 21F

MAXIMUM RATINGS

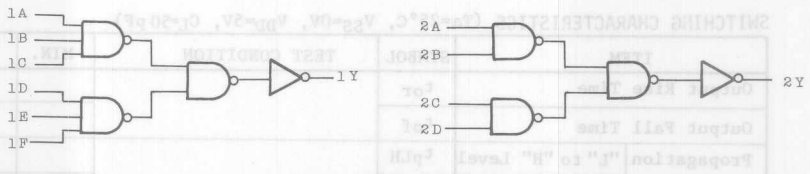
ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	Tstg	-65∿150	°C
Lead Temperature/Time	Tsol	260°C · 10sec	

TRUTH TABLE

$$1Y=\overline{(1A\cdot 1B\cdot 1C) + (1D\cdot 1E\cdot 1F)}$$

$$2Y=\overline{(2A\cdot 2B) + (2C\cdot 2D)}$$

LOGIC DIAGRAM



※ All inputs are equipped with protection circuit.

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}$, V_{DD}	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}$, V_{DD}	5	-	0.05	-	0.0	0.05	-	0.05	
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IH}=V_{SS}$, V_{DD}	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS}$, V_{DD}	5	1.4	-	1.1		-	0.8	-	
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\| < 1\mu A$ V_{OUT}=0.5V V_{OUT}=4.5V	5	4.0	-	4.0		-	4.0	-	V
	Low Level	V_{IL}		5	-	1.0	-		1.0	-	1.0	
Input Current	High Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	Low Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS}$, V_{DD}	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig. 1	-	20	40	ns
Output Fall Time		t_{of}		-	20	40	
Propagation Delay Time	"H" to "L" Level	$t_{f\,LH}$	Fig. 1	-	25	36	ns
	"L" to "H" Level	$t_{p\,HL}$		-	20	28	
Propagation Delay Time	High Level	$t_{p\,LH}$	Fig. 2	-	18	26	ns
	Low Level	$t_{p\,HL}$		-	22	30	
Input Capacitance		C_{IN}		-	5	-	pF

SWITCHING TIME TEST CIRCUITS

Fig 1.

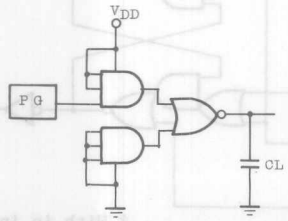
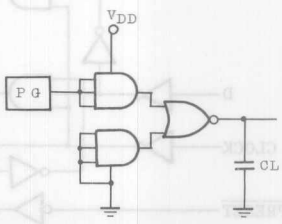


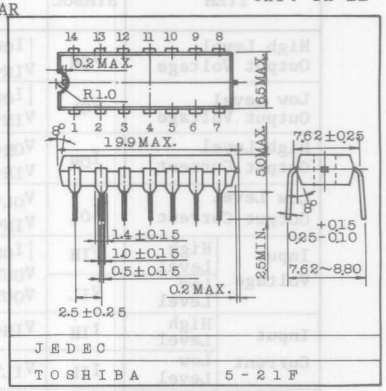
Fig 2.



"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H074P
SILICON MONOLITHIC

TENTATIVE
TC40H074P DUAL D-TYPE FLIP-FLOPS WITH PRESET AND CLEAR

Unit in mm



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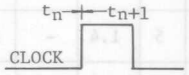
TC40H074P contains two circuits of D-type flip-flops having capabilities of clear and preset operations.

D-MODE (*1)

t_n	t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

*1...$\overline{CLEAR}$ and $\overline{PRESET}$ shall be held at "H" or "L".

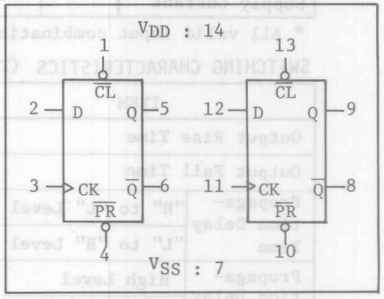


R-S MODE (*2)

INPUTS		OUTPUTS	
$\overline{CLEAR}$	$\overline{PRESET}$	$\overline{Q}$	Q
H	L	L	H
L	H	H	L
L	L	H	H
H	H	D-MODE	

*2...D and CLOCK shall be set at "H" or "L".

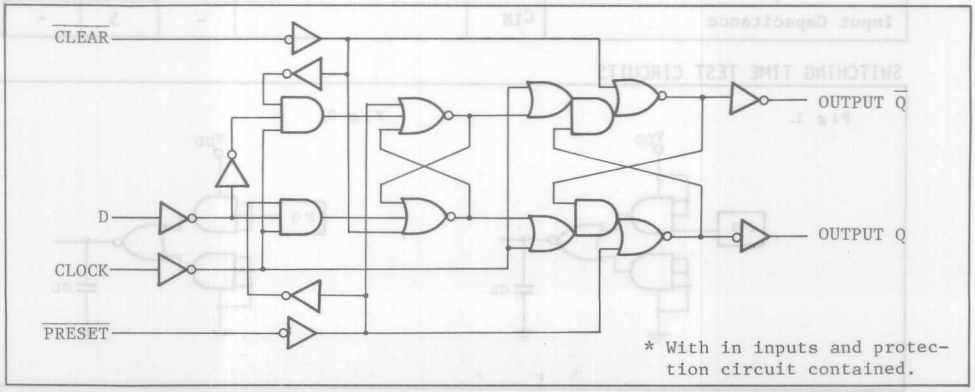
BLOCK DIAGRAM



MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temp./Time	T_{sol}	260°C·10 sec	

LOGIC DIAGRAM



* With in inputs and protection circuit contained.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0.0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05		0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1		-	0.8	-	mA
Input Voltage	High Level	V_{IN}	$\|I_{OUT}\|$ <1μA V_{OH}=4.5V V_{OL}=0.5V	5	4.0	-	4.0		-	4.0	-	V
	Low Level	V_{IL}		5	-	1.0	-		1.0	-	1.0	V
Input Current	High Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	Low Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	5.0	-	10^{-2}	5.0	-	25.0	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS} 0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}		5		27	38	ns
Output Fall Time		t_{of}		5		27	38	ns
Propagation Delay Time	(Low-High)	t_{pLH}	CLOCK-Q, $\overline{Q}$	5		49	67	ns
	(High-Low)	t_{pHL}		5		43	60	ns
Propagation Delay Time	(Low-High)	t_{pLH}	$\overline{CLEAR}$ / $\overline{PRESET}$ -Q, $\overline{Q}$	5		33	47	ns
	(High-Low)	t_{pHL}		5		59	81	ns
Minimum Pulse Width		t_w	$\overline{CLEAR}$, $\overline{PRESET}$	5		20	32	ns
Maximum clock Rise/Fall Time		$t_{r\phi}$ $t_{f\phi}$	CLOCK	5	-	-	1	μs
Minimum Data Set Up Time		t_{set-up}	D-CLOCK	5		20		ns
Input Capacitance		C_{IN}		-	-	5		pF
Maximum Clock Frequency		$f_{MAX\phi}$		5	10	20	-	MHz

"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H076P
SILICON MONOLITHIC

TENTATIVE

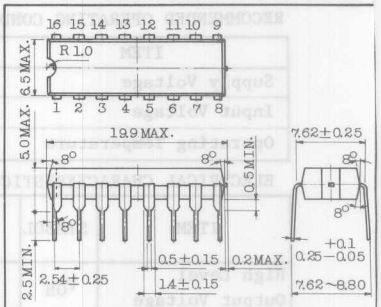
TC40H076P DUAL J-K FLIP FLOPS WITH PRESET AND CLEAR

Unit in mm

TC40H076P is J-K master-slave flip-flop having capabilities of asynchronous clear and preset Operations.

J-K Mode : When clock input is applied holding both of $\overline{CLEAR}$ and $\overline{PRESET}$ at "H" Level, the output varies according to the conditions of J and K at the trailing edge of $\overline{CLOCK}$.

R-S Mode : When $\overline{CLEAR}$ is set to "L" and $\overline{PRESET}$ to "H", Q="L" and Q="H" are obtained regardless of other inputs, and when $\overline{CLEAR}$ is set to "H" and $\overline{PRESET}$ to "L", Q="H" and Q="L" are obtained regardless of other inputs.

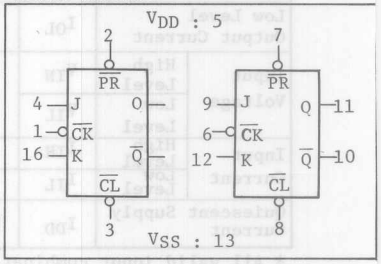


JEDEC	—
TOSHIBA	5-22E

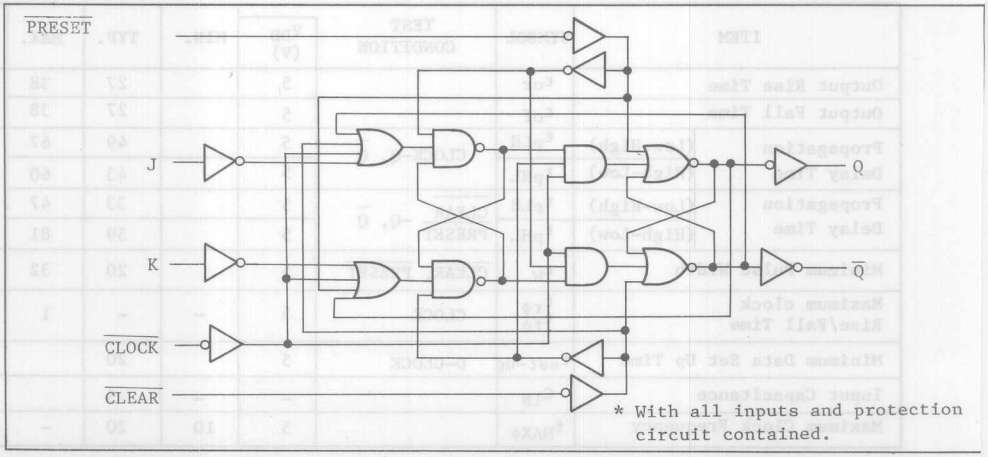
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature/Time	T_{sol}	260°C·10 sec	

BLOCK DIAGRAM



LOGIC DIAGRAM



* With all inputs and protection circuit contained.

TRUTH TABLE

INPUTS					OUTPUT	
$\overline{\text{PRESET}}$	$\overline{\text{CLEAR}}$	$\overline{\text{CLOCK}}$	J	K	Qn	$\overline{\text{Qn}}$
L	H	*	*	*	H	L
H	L	*	*	*	L	H
L	L	*	*	*	H	H
H	H	↓	L	L	NO CHANGE	
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	↑	*	*	NO CHANGE	

* : Don't Care

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0.0	-	V_{DD}	V
Operating Temperature	t_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V_{OH}	$\lvert I_{OUT}\rvert$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\lvert I_{OUT}\rvert$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current	I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1	-	-	0.8	-	mA
High Level Input Voltage	V_{IH}	$\lvert I_{OUT}\rvert$ <1μA V_{OH}=4.5V	5	4.0	-	4.0	-	-	4.0	-	V
Low Level Input Voltage	V_{IL}	V_{OL}=0.5V	5	-	1.0	-	-	1.0	-	1.0	V
High Level Input Current	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Low Level Input Current	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current	I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	5.0	-	10^{-2}	5.0	-	25.0	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_{or}		5		20	40	ns
Output Fall Time	t_{of}		5		20	40	
(Low-High) Propagation Delay Time	t_{pLH}	$\overline{\text{CLOCK}}$-Q, $\overline{Q}$	5		35		ns
(High-Low) Propagation Delay Time	t_{pHL}		5		50		
(Low-High) Propagation Delay Time	t_{pLH}	$\overline{CL}$, $\overline{PR}$-Q, $\overline{Q}$	5		35		ns
(High-Low) Propagation Delay Time	t_{pHL}		5		60		
Minimum Pulse Width	t_W	$\overline{\text{CLEAR}}$, $\overline{\text{PRESET}}$	5		25		
Maximum Clock Rise Time	$t_{r\phi}$		5	-	-	1	μs
Maximum Clock Fall Time	$t_{f\phi}$		5	-	-	1	
Minimum Data Set Up Time	t_{set-up}		5		25		ns
Maximum Clock Frequency	f-MAXϕ		5	10	20		MHz
Input Capacitance	C_{IN}				5		pF

"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H107P
SILICON MONOLITHIC

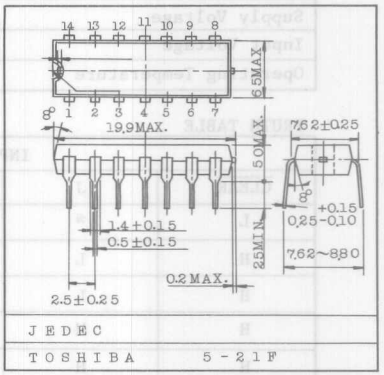
TENTATIVE

TC40H107P DUAL J-K FLIP FLOPS WITH CLEAR

Unit in mm

TC40H107P is J-K master-slave flip-flop having capabilities of asynchronous clear operations.

J-K Mode : When clock input is applied holding of $\overline{CLEAR}$ at "H" level, the output varies according to the conditions of J and K at the trailing edge of $\overline{CLOCK}$.

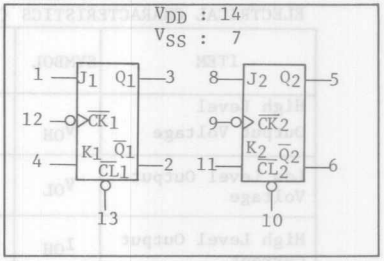


JEDEC
TOSHIBA 5-21F

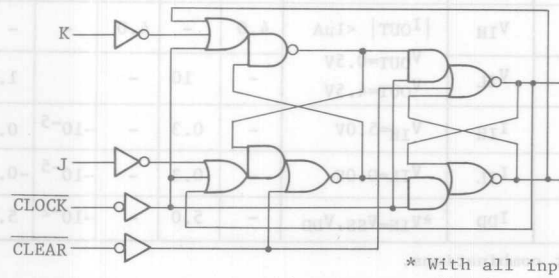
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
Input Current	V_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature/Time	T_{sol}	260°C 10·sec	

BLOCK DIAGRAM



LOGIC DIAGRAM



* With all inputs and protection circuit contained.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{CLEAR}$	J	K	$\overline{CLOCK}$	Q	$\overline{Q}$
L	*	*	*	L	H
H	L	L	↓	NO CHANGE	
H	L	H	↓	L	H
H	H	L	↓	H	L
H	H	H	↓	TOGGLE	

* Don't care

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V, V_{DD}=5.0V)

ITEM	SYMBOL	TEST CONDITION	-40°C		25°C			85°C		UNIT
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V_{OH}	$\lvert I_{OUT}\rvert$ <1μA $V_{IN}=V_{SS},V_{DD}$	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\lvert I_{OUT}\rvert$ <1μA $V_{IN}=V_{SS},V_{DD}$	-	0.05	-	0.0	0.05		0.05	
High Level Output Current	I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	1.4		1.1		-	0.8	-	
Input Voltage High Level	V_{IH}	$\lvert I_{OUT}\rvert$ <1μA V_{OUT}=0.5V V_{OUT}=4.5V	4.0	-	4.0	-	-	4.0	-	V
Input Voltage Low Level	V_{IL}		-	10	-		1.0	-	1.0	
Input Current High Level	I_{IH}	V_{IH}=5.0V	-	0.3	-	-10^{-5}	0.3	-	1.0	μA
Input Current Low Level	I_{IL}	V_{IL}=0.0V	-	0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiscent Supply Current	I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	-	5.0	-	-10^{-2}	5.0	-	30	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, V_{DD}=5.0V, C_L=15pF)

ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_{or}		-	20	40	ns
Output Fall Time	t_{of}		-	20	40	
(Low-High) Propagation Delay Time	t_{pLH}	$\overline{CLOCK}$-Q, $\overline{Q}$	-	23	36	ns
(High-Low) Propagation Delay Time	t_{pHL}		-	34	52	
(Low-High) Propagation Delay Time	t_{pLH}	$\overline{CLEAR}$-Q, $\overline{Q}$	-	24	38	ns
(High-Low) Propagation Delay Time	t_{pHL}		-	35	52	
Minimum Pulse Width	t_w	$\overline{CLOCK}$ / $\overline{CLEAR}$	-	25	40	ns
Maximum Clock Rise Time	$t_{r\phi}$		-	-	1	μs
Maximum Clock Fall Time	$t_{f\phi}$		-	-	1	
Minimum Data Set Up Time	t_{set-up}		20	25	-	ns
Maximum Clock Frequency	f-MAXϕ		10	20	-	MHz
Input Capacitance	C_{IN}		-	5	-	pF

"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H138P
SILICON MONOLITHIC

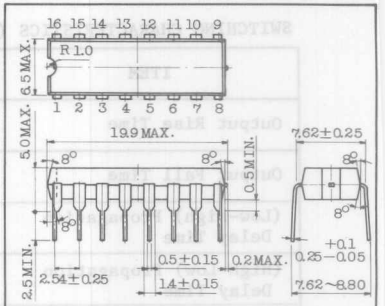
TENTATIVE

TC40H138P 3-TO-8 LINE DECODERS/MULTIPLEXERS

TC40H138P is a DECODER/MULTIPLEXER capable of selecting arbitrary one of eight outputs by three binary inputs A, B, and C, in this case, the selected output is at "H" level.

Also, when ENABLE input G1 is set to "L" level or ENABLE input G2 is set to "H" level, the selection is inhibited regardless of other input signals and all the outputs are at "H" level.

Unit in mm



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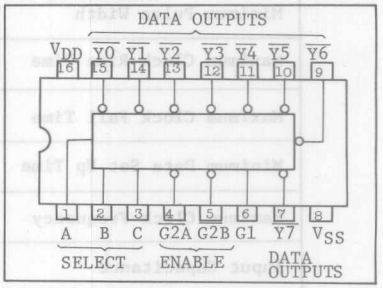
TOSHIBA	5-22E

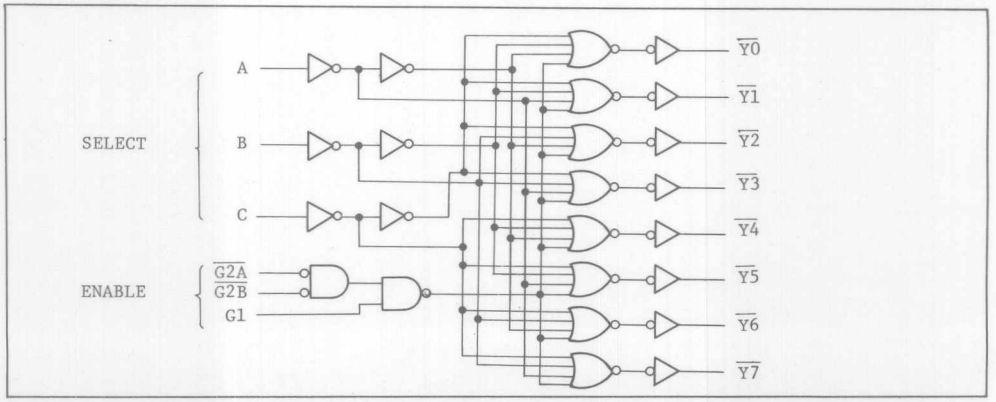
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	V_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temp./Time	T_{sol}	260°C·10 sec	

PIN CONNECTION



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITION

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	G2A	G2B	A	B	C	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L	*	*	*	*	*	H	H	H	H	H	H	H	H
*	H	*	*	*	*	H	H	H	H	H	H	H	H
*	*	H	*	*	*	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	H	L	L	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

* Don't care

ELECTRICAL CHARACTERISTICS

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\lvert I_{OUT}\rvert$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\lvert I_{OUT}\rvert$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Voltage		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1		-	0.8	-	mA
High Level Output Current		V_{IH}	$\lvert I_{OUT}\rvert$ <1μA V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
Low Level Input Voltage		V_{IL}	V_{OUT}=4.5V	5	-	1.0	-		1.0	-	1.0	V
Input Current	"H" Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Current Consumption		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	5.0	-	10^{-2}	5.0	-	30	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, CL=15pF)

ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_{or}			20	40	ns
Output Fall Time	t_{of}			20	40	
(LOW-HIGH) Propagation Delay Time	t_{pLH}	SELECT - Y		35	50	ns
(HIGH-LOW) Propagation Delay Time	t_{pHL}			40	55	
(LOW-HIGH) Propagation Delay Time	t_{pLH}	ENABLE - Y		35	50	ns
(HIGH-LOW) Propagation Delay Time	t_{pHL}			40	55	
Input Capacitance	C_{IN}		-	5	-	pF

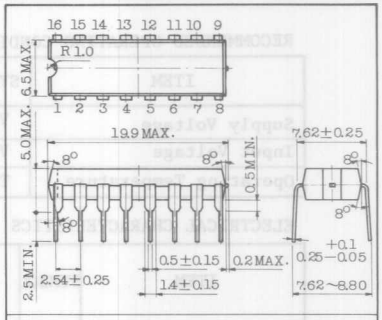
"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H139P
SILICON MONOLITHIC

TC40H139P DUAL 2-TO-4 LINE DECODERS/MULTIPLEXERS

Unit in mm

DUAL 2-TO-4 LINE DECODER/MULTIPLEXER TC40H139P is a DECODER/MULTIPLEXER including the circuits capable of selecting arbitrary one of four outputs according to the following truth table by the binary inputs A and B. In this case, the selected output is at "H" level.

Also, when ENABLE input $\overline{G}$ is set to "H" level, the selection is inhibited regardless of SELECT signal and all the outputs are at "H" level.

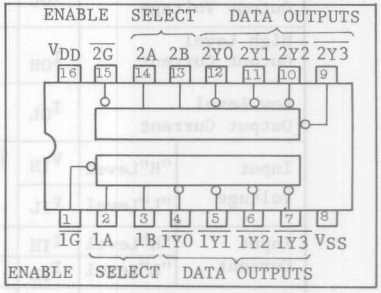


JEDEC	—
TOSHIBA	5-22E

MAXIMUM RATINGS

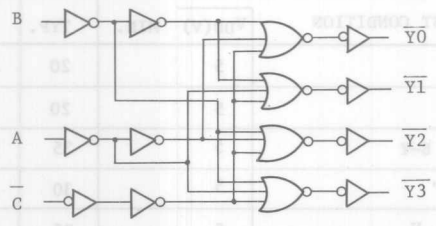
ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	-10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temp./Time	T_{sol}	260°C·10 sec	

PIN CONNECTION



LOGIC DIAGRAM

1/2 Circuit



TRUTH TABLE

INPUT			OUTPUT			
ENABLE	SELECT					
$\overline{G}$	A	B	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
H	*	*	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

* Don't care

RECOMMENDED OPERATING CONDITION

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0.0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage		V_{OH}	$\|V_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|V_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05		0.05	V
High Level Output Current		I_{OH}	$V_{OH}=4.6V$ $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	$V_{OL}=0.4V$ $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1		-	0.8	-	mA
Input Voltage	"H"Level	V_{IH}	$\|V_{OUT}\| < 1\mu A$ $V_{OH}=4.5V$	5	4.0	-	4.0		-	4.0	-	V
	"L"Level	V_{IL}	$V_{OL}=0.5V$	5	-	1.0	-		1.0	-	1.0	V
Input Current	"H"Level	I_{IH}	$V_{IH}=5.0V$	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L"Level	I_{IL}	$V_{IL}=0.0V$	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Current Consumption		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	5.0	-	10^{-2}	5.0	-	30	μA

* All valid input combinations

SWITHCING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_r		5		20	40	ns
Output Fall Time		t_f		5		20	40	ns
(LOW→HIGH)	Propagation Delay Time	t_{pLH}	A, B-Y	5		35	50	ns
(HIGH→LOW)		t_{pHL}	"	5		30	45	ns
(LOW→HIGH)	Propagation Delay Time	t_{pLH}	$\overline{G}$ - Y	5		35	50	ns
(HIGH→LOW)		t_{pHL}	"	5		30	45	ns
Input Capacitance		C_{IN}				5		pF

"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H153P
SILICON MONOLITHIC

TC40H153P DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

Unit in mm

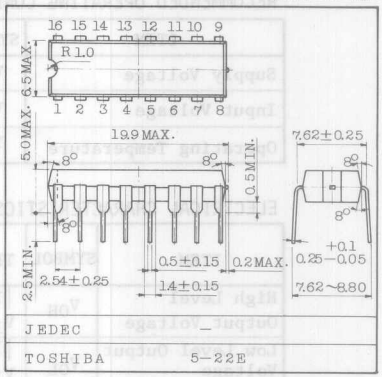
TC40H153P is a data selector with two circuits that selects the four data by means of common select inputs A and B.

The 4-channel data of C_0 - C_3 are selected to OUTPUT 1Y or OUTPUT 2Y according to SELECT A or SELECT B.

Each output becomes "L" level regardless of other inputs by setting STROBE input at "H" level.

This TC40H153P can be widely applied to the signal composition, parallel to serial conversion, and selection of various signals.

The pin assignments and functions of TC40H153P are the same as those of LSTTL 74LS153.

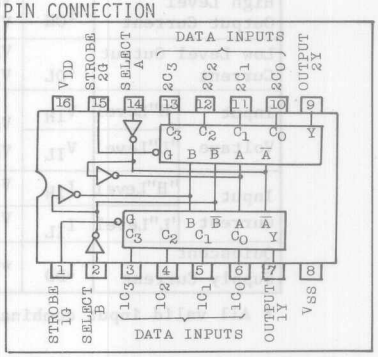


JEDEC —
TOSHIBA 5-22E

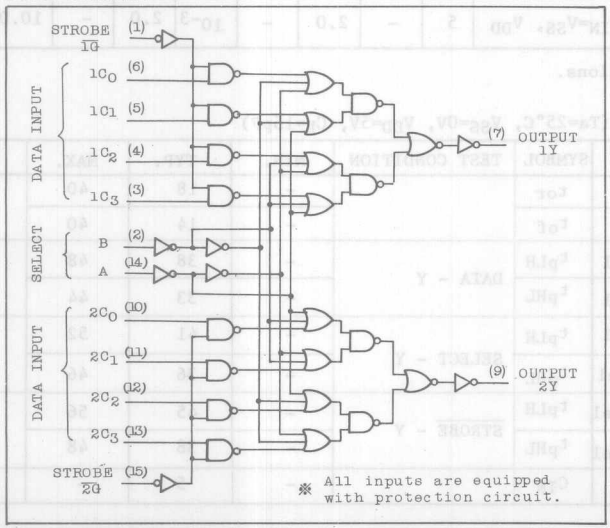
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS} -0.5 ∿ V_{SS} +10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature/Time	T_{sol}	260°C·10 sec	

PIN CONNECTION



LOGIC DIAGRAM



※ All inputs are equipped with protection circuit.

TRUTH TABLE

INPUTS							OUTPUTS
SELECT		DATA				STROBE	
A	B	C_0	C_1	C_2	C_3	$\overline{G}$	Y
※	※	※	※	※	※	H	L
L	L	L	※	※	※	L	L
L	L	H	※	※	※	L	H
H	L	※	L	※	※	L	L
H	L	※	H	※	※	L	H
L	H	※	※	L	※	L	L
L	H	※	※	H	※	L	H
H	H	※	※	※	L	L	L
H	H	※	※	※	H	L	H

※ = Don't Care

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}, V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}, V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current	I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS}, V_{DD}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS}, V_{DD}$	5	1.4	-	1.1		-	0.8	-	mA
Input Voltage "H"Level	V_{IH}	$\|I_{OUT}\|$= < 1μA V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
Input Voltage "L"Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-		1.0	-	1.0	V
Input Current "H"Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L"Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current	I_{DD}	*$V_{IN}=V_{SS}, V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}		-	18	40	ns
Output Fall Time		t_{of}		-	14	40	ns
Propagation Delay Time	Low to High Level	t_{pLH}	DATA - Y	-	38	48	ns
	High to Low Level	t_{pHL}		-	33	44	ns
Propagation Delay Time	Low to High Level	t_{pLH}	SELECT - Y	-	41	52	ns
	High to Low Level	t_{pHL}		-	36	46	ns
Propagation Delay Time	Low to High Level	t_{pLH}	$\overline{STROBE}$ - Y	-	45	56	ns
	High to Low Level	t_{pHL}		-	38	48	ns
Input Capacitance		C_{IN}		-	5	-	PF

Toshiba **INTEGRATED CIRCUIT**

TECHNICAL DATA

"C²MOS" DIGITAL INTEGRATED CIRCUIT

TC40H155P

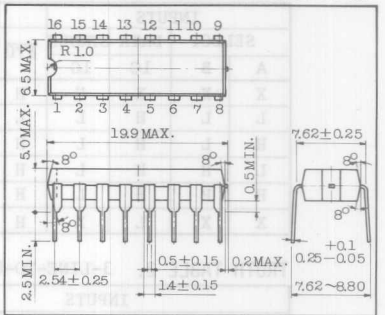
SILICON MONOLITHIC

TC40H155P DUAL 2-LINE-TO-4-LINE DECODER/DEMULTIPLEXERS

TC40H155P is a decoder/demultiplexers containing two circuits. When STROBE = "L", arbitrary one of four outputs can be selected by the two common binary inputs A and B. And the selected output becomes "H" level. When STROVE = "H" selection is inhibited and all the outputs become "H" level regradless of other input signals.

By combining with each input, TC40H155P can be used as 3-LINE-TO-8-LINE DECODER or 1-LINE-TO-8-LINE-DEMULTIPLEXER. In this case, refer to TRUTH TABLE for each input condition.

Unit in mm

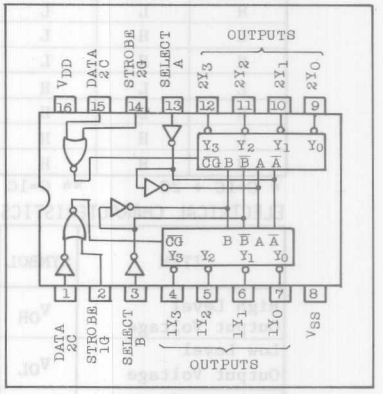


JEDEC	—
TOSHIBA	5-22E

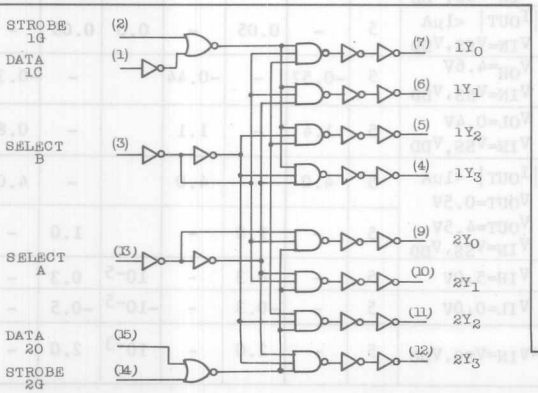
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS} + 10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD} + 0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD} + 0.5	V
Input Current	I_{IN}	10	mA
Power Dissipation	P_D	±300	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature/Time	T_{sol}	260°C · 10sec	

PIN CONNECTION



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	2.0	-	8.0	V
Input Voltage	V_{IN}	0	-	VDD	V
Operating Temperature	T_{opr}	-40	-	85	℃

※ All inputs are equipped with protection circuit.

TRUTH TABLE 1. 2-LINE-TO-4-LINE DECODER or 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		DATA	STROBE				
A	B	1C	1G	$\overline{1Y0}$	$\overline{1Y1}$	$\overline{1Y2}$	$\overline{1Y3}$
X	X	X	H	H	H	H	H
L	L	H	L	L	H	H	H
H	L	H	L	H	L	H	H
L	H	H	L	H	H	L	H
H	H	H	L	H	H	H	L
X	X	L	X	H	H	H	H

INPUTS				OUTPUTS			
SELECT		DATA	STROBE				
A	B	2C	2G	$\overline{2Y0}$	$\overline{2Y1}$	$\overline{2Y2}$	$\overline{2Y3}$
X	X	X	H	H	H	H	H
L	L	L	L	L	H	H	H
H	L	L	L	H	L	H	H
L	H	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	H	X	H	H	H	H

X=Don't care

TRUTH TABLE 2. 3-LINE-TO-8-LINE DECODER or 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
A	B	* C	** G	$\overline{2Y0}$	$\overline{2Y1}$	$\overline{2Y2}$	$\overline{2Y3}$	$\overline{1Y0}$	$\overline{1Y1}$	$\overline{1Y2}$	$\overline{1Y3}$
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

* C=1C + 2C ** G=1G + 2G X=Don't care

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\lvert I_{OUT}\rvert$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\lvert I_{OUT}\rvert$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current	I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1		-	0.8	-	mA
High Level Input Voltage	V_{IH}	$\lvert I_{OUT}\rvert$ <1μA V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
Low Level Input Voltage	V_{IL}	V_{OUT}=4.5V $V_{IN}=V_{SS},V_{DD}$	5	-	1.0	-		1.0	-	1.0	V
Input Current "H" Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.5	-	-1.0	μA
Quiescent Supply Current	I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}		-	17	40	ns
Output Fall Time		t_{of}		-	12	30	
Propagation Delay Time	Low to High Level	t_{pLH}	SELECT A - $\overline{Y}$	-	35		ns
	High to Low Level	t_{pHL}	SELECT B	-	31		
Propagation Delay Time	Low to High Level	t_{pLH}	STROBE 1G - $\overline{Y}$ STROBE 2G	-	32		ns
	High to Low Level	t_{pHL}		-	27		
Propagation Delay Time	Low to High Level	t_{pLH}	DATA 1C - $\overline{Y}$	-	32		ns
	High to Low Level	t_{pHL}		-	27		
Propagation Delay Tiem	Low to High Level	t_{pLH}	DATA 2C - $\overline{Y}$	-	32		ns
	High to Low Level	t_{pHL}		-	27		
Input Capacitance		C_{IN}		-	5	-	PF

"C²MOS" DIGITAL INTEGRATED CIRCUIT

TC40H157P TC40H158P

SILICON MONOLITHIC

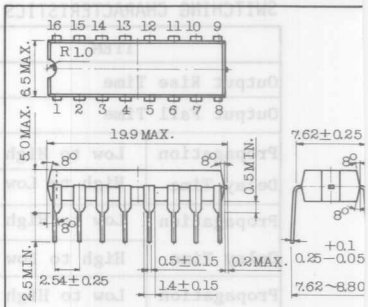
TC40H157P QUAD 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS.
TC40H158P QUAD 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS.

TC40H157P/158P is a data selector with four circuits that selects the two data inputs A and B by means of SELECT input. The SELECT input is common to the four circuits.

The data A is selected by setting STROBE input and SELECT input at "L" levels, and the data B is selected by setting SELECT input at "H" level.

When STROBE input is set at "H" level, selection is inhibited regardless of other inputs; as a result, all the outputs of TC40H157P become "L" level, and all the outputs of TC40H158P become "H" level.

Unit in mm



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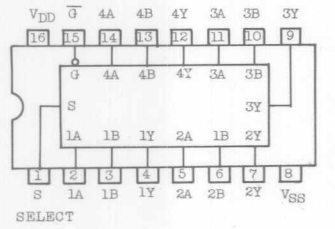
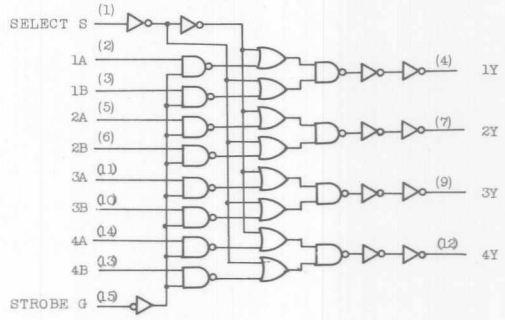
TOSHIBA	5−22E

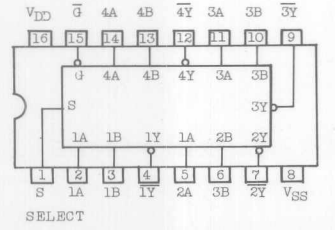
PIN CONNECTION AND LOGIC DIAGRAM

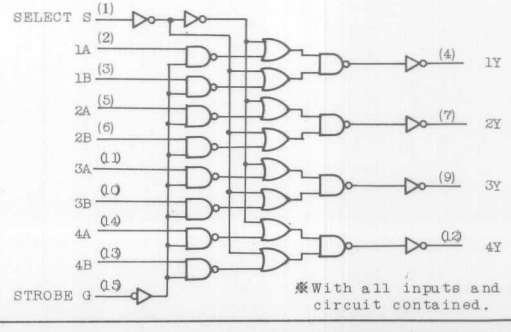
TC40H157P





TC40H158P





※With all inputs and protection circuit contained.

MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature/Time	T_{sol}	260°C · 10sec	

TRUTH TABLE

INPUTS				OUTPUTS	
STROBE	SELECT	DATA		H157P	H158P
G	S	A	B	Y	Y
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X=Don't care

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V, V_{DD}=5V)

ITEM	SYMBOL	TEST CONDITION	-40°C		25°C			80°C		UNIT
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS},V_{DD}	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA V_{IN}=V_{DD},V_{SS}	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current	I_{OH}	V_{OH}=4.6V V_{IN}=V_{SS},V_{DD}	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V V_{IN}=V_{DD},V_{SS}	1.4	-	1.1	-	-	0.8	-	mA
High Level Input Voltage	V_{IH}	$\|I_{OUT}\|$<1μA V_{OUT}=0.5V	4.0	-	4.0	-	-	4.0	-	V
Low Level Input Voltage	V_{IL}	V_{OUT}=4.5V	-	1.0	-	-	1.0	-	1.0	V
High Level Input Current	I_{IH}	V_{IH}=5.0V	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Low Level Input Current	I_{IL}	V_{IL}=0.0V	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current	I_{DD}	*V_{IN}=V_{SS},V_{DD}	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=15pF)

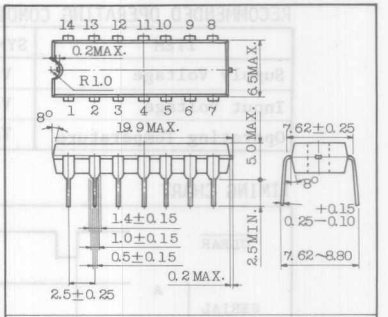
ITEM		SYMBOL	TEST CONDITION	TC40H157P			TC40H158P			UNIT
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Rise Time		t_{or}		-	18	40	-	17	40	ns
Output Fall Time		t_{of}		-	15	40	-	15	40	
Propagation Delay Time	"L" to "H" Level	t_{pLH}	DATA - Y, $\overline{Y}$	-	26	36	-	25	36	ns
	"H" to "L" Level	t_{pHL}		-	29	40	-	22	32	
Propagation Delay Time	"L" to "H" Level	t_{pLH}	SELECT - Y, $\overline{Y}$	-	34	44	-	27	34	ns
	"H" to "L" Level	t_{pHL}		-	32	42	-	30	40	
Propagation Delay Time	"L" to "H" Level	t_{pLH}	STROBE - Y, $\overline{Y}$	-	33	44	-	26	36	ns
	"H" to "L" Level	t_{pHL}		-	31	42	-	28	38	
Input Capacitance		C_{IN}		-	5	-	-	5	-	pF

"C²MOS" DIGITAL INTEGRATED CIRCUIT

TC40H164P

SILICON MONOLITHIC

Unit in mm



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TOSHIBA	5-21F

TC40H164P 8-BIT SHIFT REGISTER (SERIAL-IN PARALLEL-OUT)

TC40H164P is a SERIAL-IN/PARALLEL-OUT shift register.

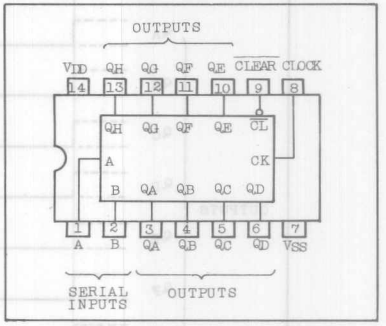
For the type D flip-flop of each stage, CLOCK input and CLEAR input are respectively common, thus being capable of performing asynchronously clear operation from the outside at arbitrary time. In this case, all the data outputs of Q become "L" levels regardless of other inputs by setting CLEAR input at "L" level.

The flip-flop of each stage is triggered at the time of the rising edge of CLOCK inputs.

MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+10$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature/Time	T_{sol}	260°C · 10sec	

PIN CONNECTION

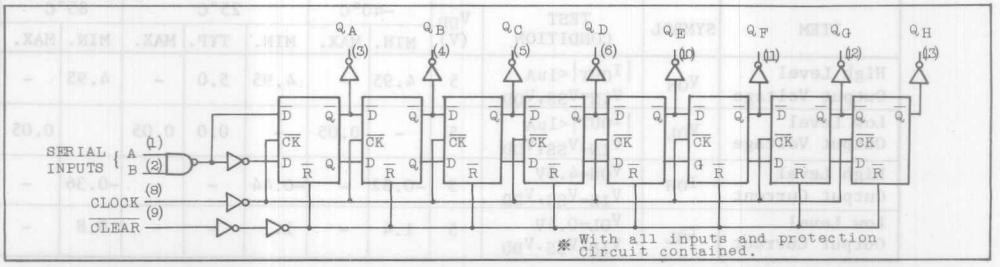


TRUTH TABLE

INPUTS				OUTPUTS							
CLEAR	CLOCK	A	B	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G	Q_H
L	X	X	X	L	L	L	L	L	L	L	L
H	L	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}	Q_{EO}	Q_{FO}	Q_{GO}	Q_{HO}
H	↑	H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}

X = Don't care

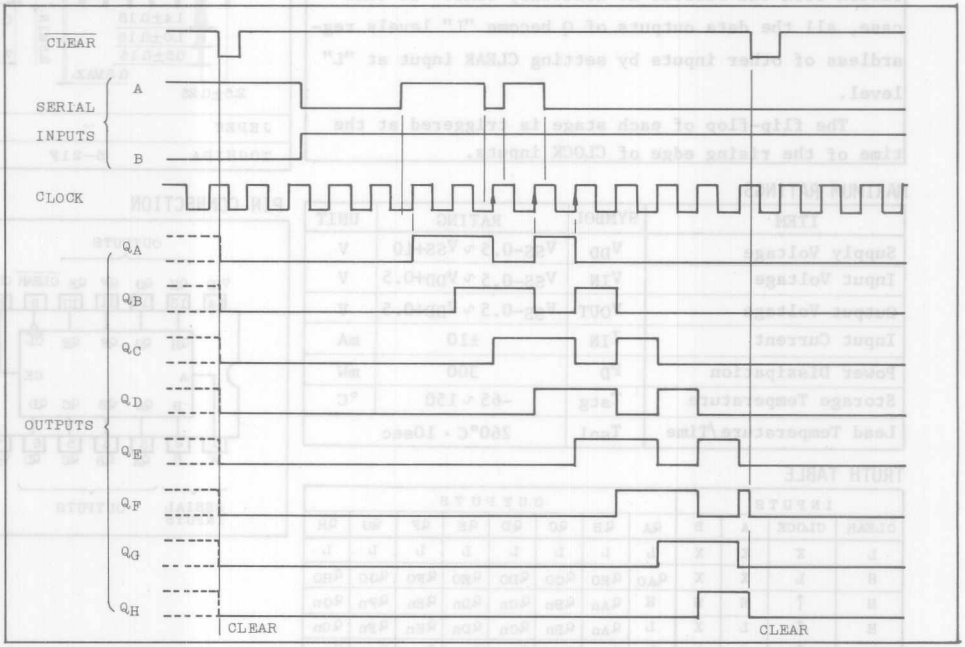
BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

TIMING CHART



ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05		0.05	V
High Level Output Current	I_{OH}	V_{OH}=4.6V $V_{IH}=V_{SS},V_{DD}$	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS}\cdot V_{DD}$	5	1.4	-	1.1	-	-	0.8	-	mA

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Input Voltage	V_{IH}	$\|I_{OUT}\|$<1μA V_{OUT}=0.5V	5	4.0	-	4.0	-	-	4.0	-	V
Low Level Input Voltage	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-	-	1.0	-	1.0	
High Level Input Current	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Low Level Input Current	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current	I_{DD}	*V_{IN}=V_{SS},V_{DD}	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=15pF)

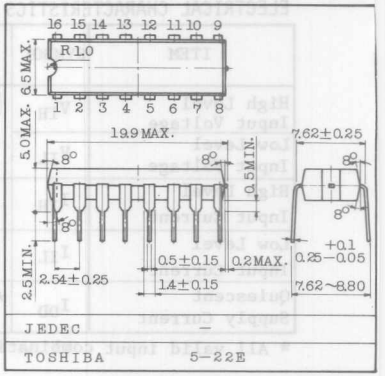
ITEM		SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}			-	20	40	ns
Output Fall Time		t_{of}			-	20	40	
Propagation Delay Time	Low to High Level	t_{pLH}	CLOCK - Q		-	45		ns
	High to Low Level	t_{pHL}			-	43		
Propagation Delay Time	Low to High Level	t_{pLH}	$\overline{CLEAR}$ - Q	CLOCK="H"	-	43		ns
	High to Low Level	t_{pHL}		CLOCK="L"	-	46		
Minimum Data Set up Time		t_{set-up}			-	15		ns
Mimimum Clear Removal Time		t_{rem}			-	15		ns
Minimum Clock Rise/Fall Time		$t_{r\phi}$ $t_{f\phi}$			-	-	1	μs
Maximum Pulse Width		$f_{max\phi}$			10	20	-	MHz
Minimum Pulse Width		t_W	CLOCK, $\overline{CLEAR}$		-	30		ns
Input Capacitance		C_{IN}			-	5	-	PF

"C²MOS" DIGITAL INTEGRATED CIRCUIT

TC40H166P

SILICON MONOLITHIC

Unit in mm



TC40H166P 8-BIT SHIFT REGISTER (S/P-IN P-OUT)

TC40H166P is an 8-bit PARALLEL-IN/SERIAL-OUT shift register, which can also perform SERIAL-IN/SERIAL-OUT operation.

In case of PARALLEL operation, the DATA of PARALLEL IN operation are output from the final stage of F/F after having been shifted in order at the rising edge of CLOCK.

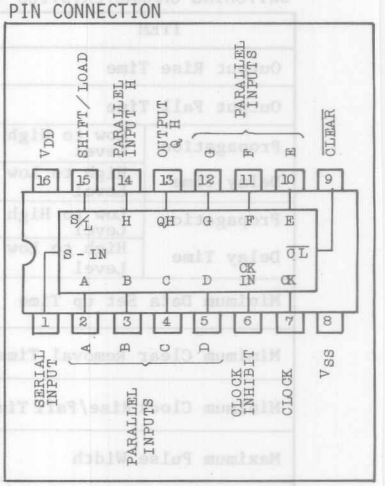
So with SERIAL OPERATION: that is, each F/F is triggered at the rising edge of CLOCK.

Shifting of PARALLEL operation and SERIAL operation can be achieved by SHIFT/LOAD input.

SERIAL operation is performed when SHIFT/LOAD inputis at "H", and PARALLEL operation is performed when it is at "L".

For detailed operation, refer to the truth table and the timing chart. The functions and pin assignments of TC40H166P are the same as those of 74LS166.

PIN CONNECTION



MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature/Time	T_{sol}	260°C · 10sec	

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

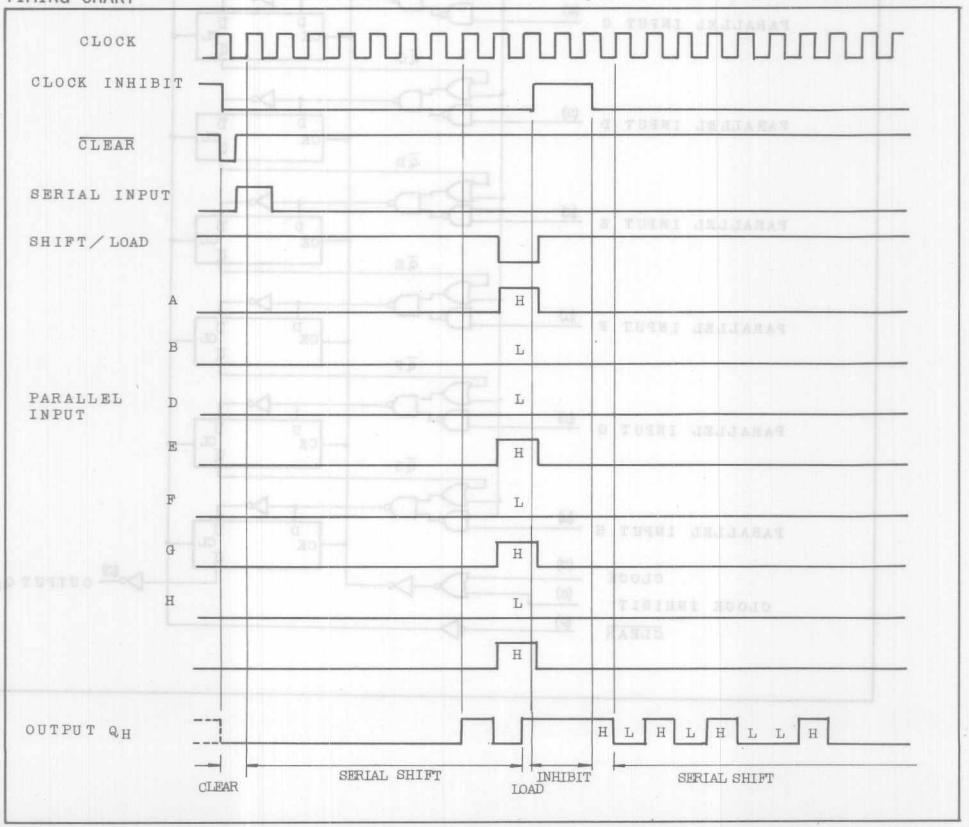
ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

TRUTH TABLE

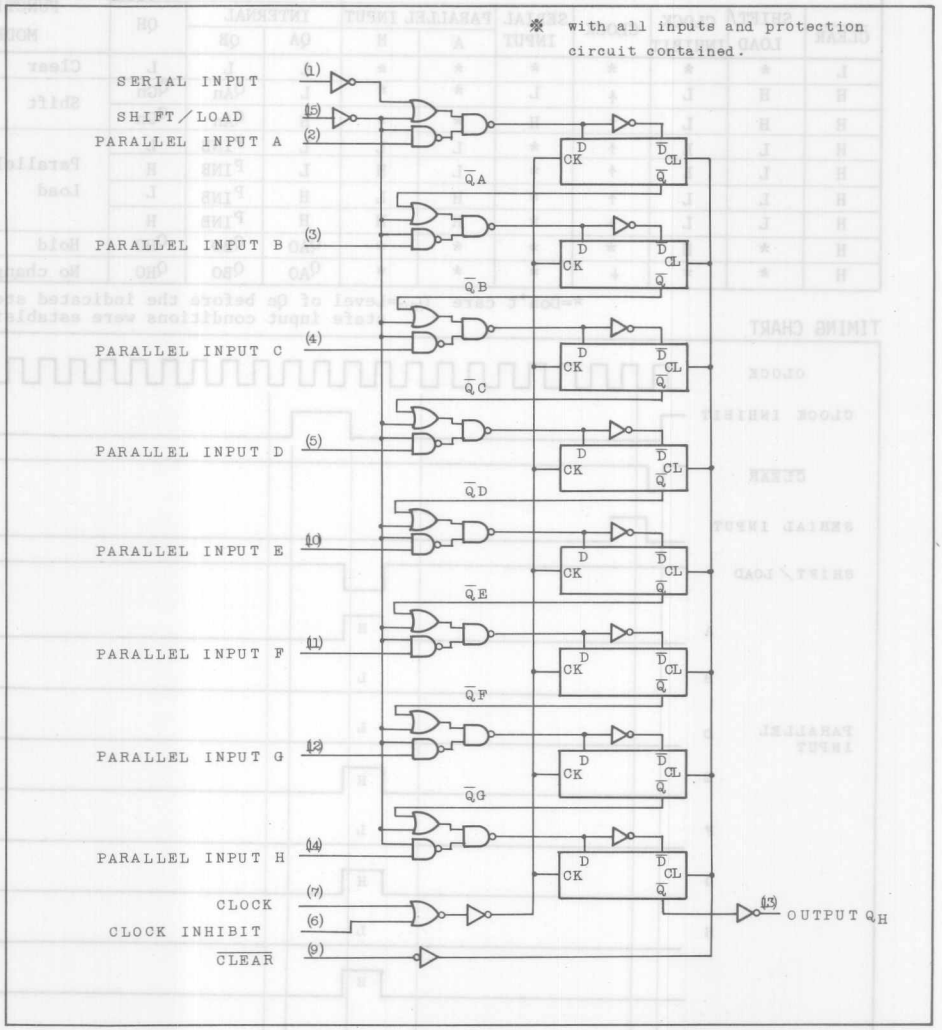
INPUTS							OUTPUTS			FUNCTION MODE
					PARALLEL INPUT		INTERNAL			
$\overline{\text{CLEAR}}$	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL INPUT	A	H	QA	QB	QH	
L	*	*	*	*	*	*	L	L	L	Clear
H	H	L	↑	L	*	*	L	Q_{An}	Q_{Gn}	Shift
H	H	L	↑	H	*	*	H	Q_{An}	Q_{Gn}	
H	L	L	↑	*	L	L	L	P_{INB}	L	Parallel Load
H	L	L	↑	*	L	H	L	P_{INB}	H	
H	L	L	↑	*	H	L	H	P_{INB}	L	
H	L	L	↑	*	H	H	H	P_{INB}	H	
H	*	H	*	*	*	*	Q_{AO}	Q_{BO}	Q_{HO}	Hold
H	*	*	↓	*	*	*	Q_{AO}	Q_{BO}	Q_{HO}	No change

*=Don't care Q_{no}=Level of Qn before the indicated steady-stafe input conditions were establsiled.

TIMING CHART



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1	-	-	0.8	-	mA
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\| < 1\mu A$ V_{OUT}=0.5V	5	4.0	-	4.0	-	-	4.0	-	V
	Low Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-	-	1.0	-	1.0	V
Input Current	High Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	Low Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	10	2.0	-	10.0	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=15pF)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time	tor		-	17	30	ns
Output Fall Time	tof		-	14	26	ns
High to Low Level Propagation Time	tpLH	CLOCK - Q_H	-	29	41	ns
Low to High Level Propagation Time	tpHL	CLOCK - Q_H	-	36	50	ns
Low to High Level Propagation Time	tpHL	CLEAR - Q_H	-	38	52	ns
Maximum Clock Frequency	$f_{max\phi}$		15	25	-	MHz

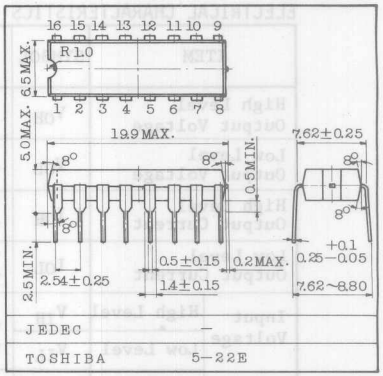
"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H174P
SILICON MONOLITHIC

TENTATIVE

Unit in mm

TC40H174P HEX "D" TYPE FLIP FLOPS

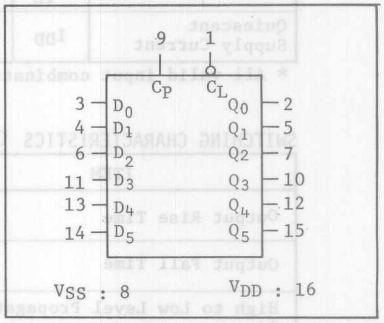
TC40H174P contains six circuits of D type flip-flop having the common clock and the common clear terminal.
The logical inputs applied to D inputs are transferred to Q outputs at the rising edge of CLOCK input.
The clear input is "L" level active.
This has the same pin connection and the same functions as TTL74174 and TC40174BP is also same.



TRUTH TABLE * Don't care

INPUTS			OUTPUT
CLOCK	D_n	$\overline{CLEAR}$	Q_n
↑	H	H	H
↑	L	H	L
↓	*	H	No change
*	*	L	L

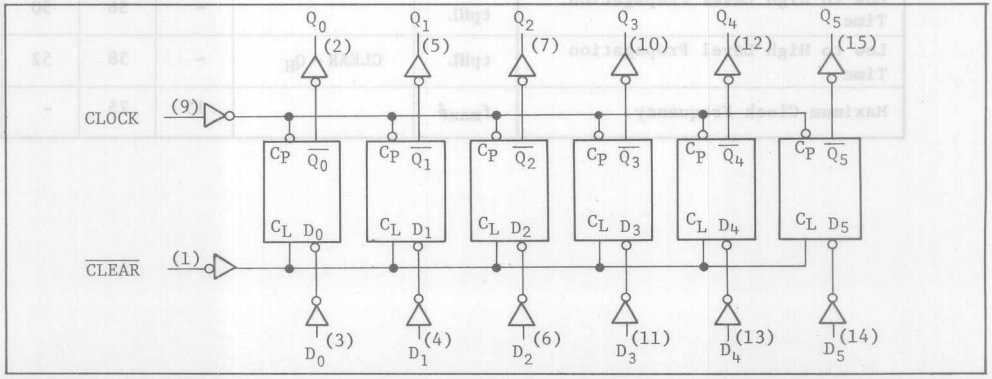
BLOCK DIAGRAM



MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{DD}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temp.	T_{stg}	-65∿150	°C
Lead Temp./Time	T_{sol}	260°C·10 sec	

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	2.0	-	8.0	V
Input Voltage	V_{IN}	0.0	-	V_{DD}	V
Operating Temp.	T_{opr}	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

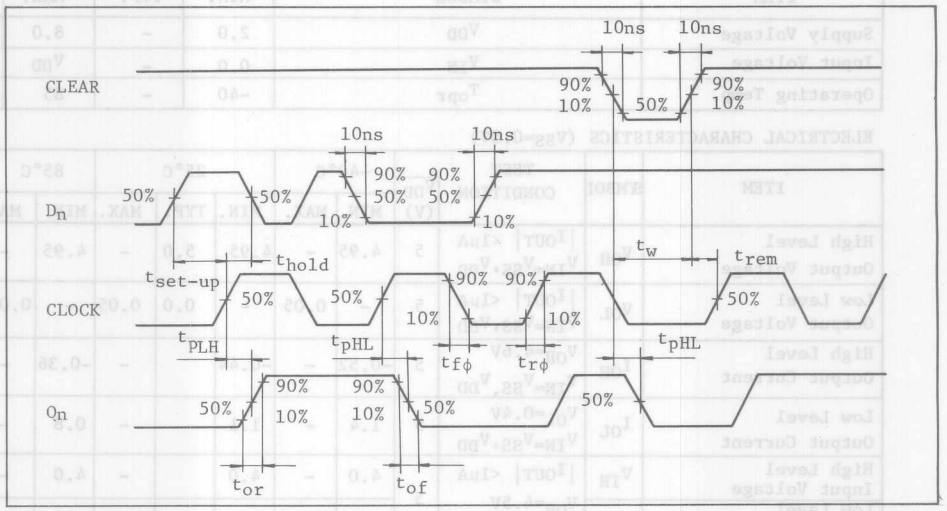
ITEM	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current	I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1		-	0.8	-	mA
High Level Input Voltage	V_{IH}	$\|I_{OUT}\|$ <1μA V_{OH}=4.5V V_{OL}=0.5V	5	4.0	-	4.0		-	4.0	-	V
Low Level Input Voltage	V_{IL}			-	1.0	-		-	1.0	1.0	V
Input Current "H" Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current	I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	20.0	-	0.005	20.0	-	150	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}		5		20	40	ns
Output Fall Time		t_{of}		5		20	40	ns
Propagation Delay	(L-H)	t_{pLH}	CLOCK-Q	5		50		ns
	(H-L)	t_{pHL}				40		
	(H-L)	t_{pHL}	$\overline{CLEAR}$-Q	5		40		ns
Min. $\overline{Clear}$ Pulse Width		t_w	$\overline{CLEAR}$	5		25		ns
Max. Clock Rise Time		$t_{r\phi}$		5			1000	ns
Max. Clock Fall Time		$t_{f\phi}$					1000	
Min. Data Set Up Time		t_{set-up}	D_n-CLOCK	5		20		ns
Max. Clock Frequency		MAXφ		5	10	20		MHz
Input Capacitance		C_{IN}				5		pF

SWITCHING TIME TEST WAVEFORM



"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H175P
SILICON MONOLITHIC

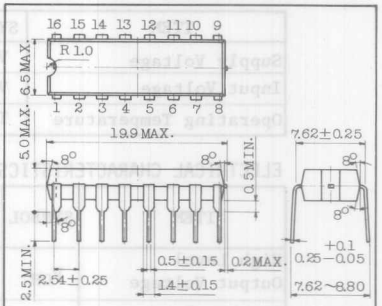
40H175P QUAD "D" TYPE FLIP-FLOPS

TC40H175P is a "D" type flip-flop with four circuits that has common CLOCK and $\overline{CLEAR}$ inputs.

The logical input applied to DATA input is transmitted to Q and $\overline{Q}$ outputs by the rising edge of CLOCK input.

If $\overline{CLEAR}$ input is set at "L" level, output Q = L level and output $\overline{Q}$ = H level regardless of other inputs.

Unit in mm



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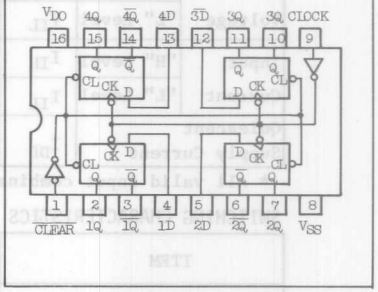
TOSHIBA	5-22E

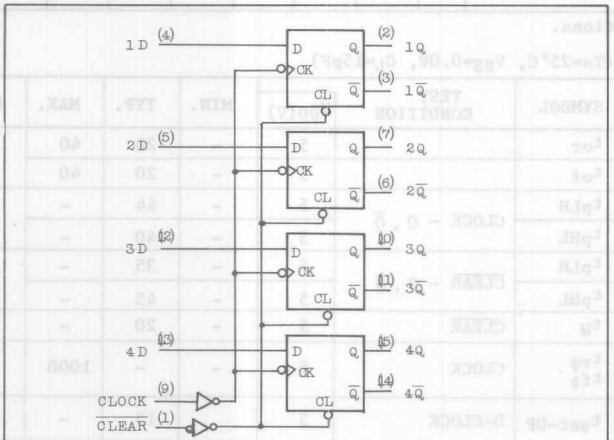
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature/Time	T_{sol}	260°C · 10sec	

PIN CONNECTION



LOGIC DIAGRAM



※ With all inputs and protection circuit contained.

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{CLEAR}$	CLOCK	DATA	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	↓	X	No Change	

X = Don't Care

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\lvert I_{OUT}\rvert$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\lvert I_{OUT}\rvert$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1		-	0.8	-	mA
Input Voltage	"H" Level	V_{IH}	$\lvert I_{OUT}\rvert$ <1μA V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
	"L" Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-		1.0	-	1.0	V
Input Current	"H" Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}		5	-	20	40	ns
Output Fall Time		t_{of}		5	-	20	40	ns
Propagation Delay Time	"L" to "H" Level	t_{pLH}	CLOCK - Q, $\bar{Q}$	5	-	44	-	ns
	"H" to "L" Level	t_{pHL}		5	-	40	-	ns
	"L" to "H" Level	t_{pLH}	$\overline{CLEAR}$ - Q, $\bar{Q}$	5	-	35	-	ns
	"H" to "L" Level	t_{pHL}		5	-	45	-	ns
Minimum Pulse Width		t_W	$\overline{CLEAR}$	5	-	20	-	ns
Maximum Clock Rise/Fall Time		$t_{r\phi}$ $t_{f\phi}$	CLOCK	5	-	-	1000	ns
Minimum Data Set up Time		t_{set-UP}	D-CLOCK	5		15	-	ns
Input Capacitance		C_{IN}		-	-	5	-	pF
Maximum Clock Frequency		f_{MAX}		5	10	20	-	MHz

Toshiba

INTEGRATED CIRCUIT

TECHNICAL DATA

"C²MOS" DIGITAL INTEGRATED CIRCUIT

TC40H192P, TC40H193P

SILICON MONOLITHIC

TENTATIVE

TC40H192P SYNCHRONOUS 4-BIT BCD UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

TC40H193P SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

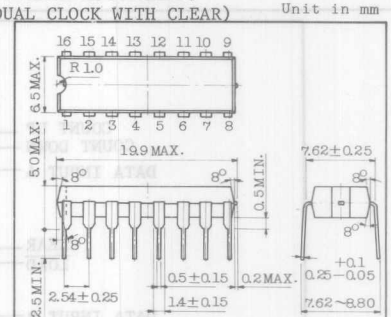
Unit in mm

TC40H192P and TC40H193P are synchronous 4-bit up/down counters.

Clear input is "H" level active and preset input is "L" level active, and both inputs functions asynchronously.

The clocks are separately provided for the up count input and for the down count input, and the rising edge of both pulses initiates the counting operations. Since the clock in the counter is obtained by logically adding the up count input and the down count input, one of clock inputs can be used as the clock inhibit input.

TC40H192P and TC40H193P are same function as TIL 74192 and 74193 and pin-to-pin compatible with those TC40192BP and TC40193BP are also same.

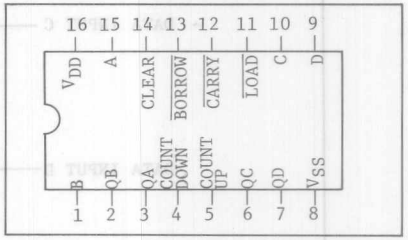


JEDEC	—
TOSHIBA	5-22E

MAXIMUM RATINGS

ITEM	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{SS}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{SS}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temp.	T_{stg}	-65∿150	°C
Lead Temp./Time	T_{sol}	260°C·10 sec	

PIN CONNECTION



TRUTH TABLE

TC40H192P/192P

COUNT UP	COUNT DOWN	$\overline{LOAD}$	CLEAR	ACTION
⎍	H	H	L	COUNT UP
⎏	H	H	L	NO COUNT
H	⎍	H	L	COUNT DOWN
H	⎏	H	L	NO COUNT
*	*	L	L	PRESET
*	*	*	H	RESET

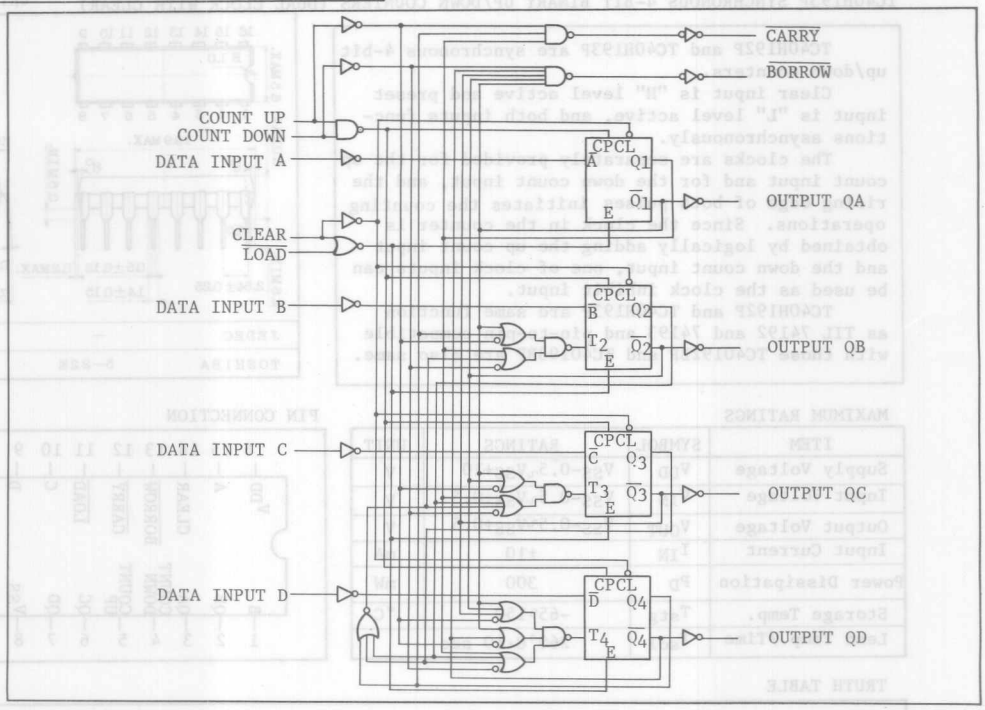
* Don't care

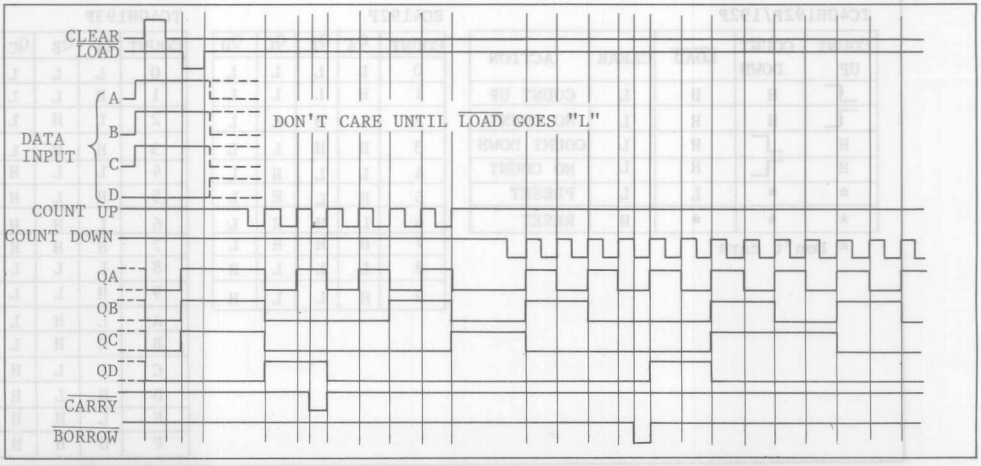
EC4192P

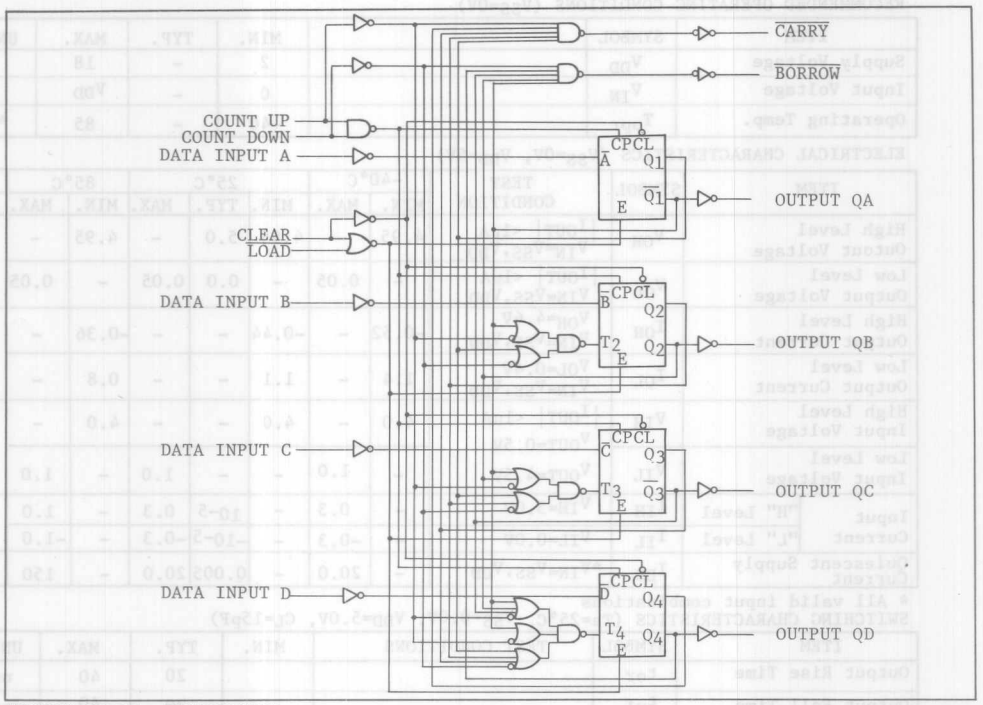
COUNT	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

TC40H193P

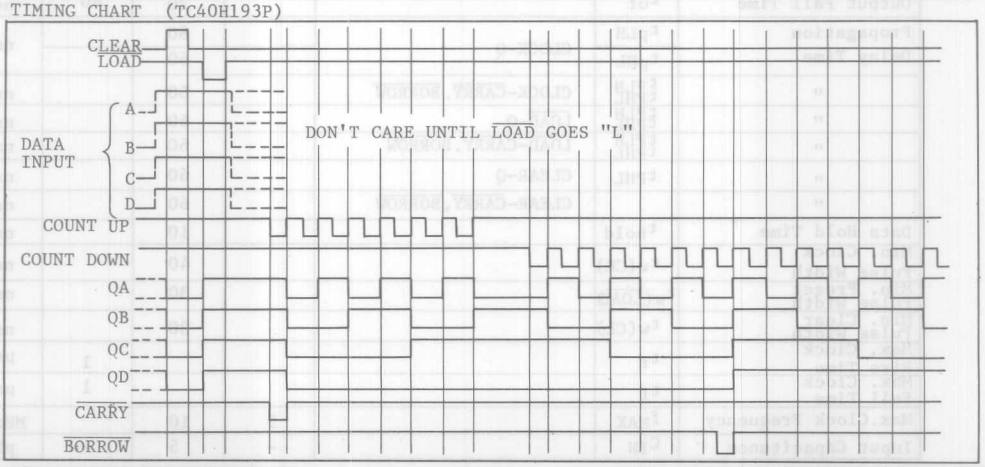
COUNT	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
A	L	H	L	H
B	H	H	L	H
C	L	L	H	H
D	H	L	H	H
E	L	H	H	H
F	H	H	H	H


CARRY
BORROW
COUNT UP
COUNT DOWN
DATA INPUT A
CLEAR
LOAD
DATA INPUT B
DATA INPUT C
DATA INPUT D
CPCL
A
Q1
E
OUTPUT QA
B
Q2
T2
OUTPUT QB
C
Q3
T3
OUTPUT QC
D
Q4
T4
OUTPUT QD


CLEAR
LOAD
DATA INPUT
A
B
C
D
DON'T CARE UNTIL LOAD GOES "L"
COUNT UP
COUNT DOWN
QA
QB
QC
QD
CARRY
BORROW



TIMING CHART (TC40H193P)



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temp.	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V, V_{DD}=5V)

ITEM		SYMBOL	TEST CONDITION	-40°C		25°C			85°C		
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	MAX.
High Level Outout Voltage		V_{OH}	$\lvert I_{OUT}\rvert$ <1μA $V_{IN}=V_{SS},V_{DD}$	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\lvert I_{OUT}\rvert$ <1μA $V_{IN}=V_{SS},V_{DD}$	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	1.4	-	1.1	-	-	0.8	-	mA
High Level Input Voltage		V_{IH}	$\lvert I_{OUT}\rvert$ <1μA V_{OUT}=0.5V	4.0	-	4.0	-	-	4.0	-	V
Low Level Input Voltage		V_{IL}	V_{OUT}=4.5V	-	1.0	-	-	1.0	-	1.0	V
Input Current	"H" Level	I_{IH}	V_{IH}=5.0V	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	-	20.0	-	0.005	20.0	-	150	μA

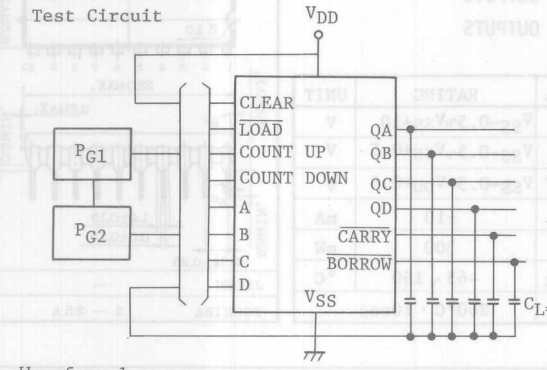
* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, V_{DD}=5.0V, C_L=15pF)

ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_{or}			20	40	ns
Output Fall Time	t_{of}			20	40	ns
Propagation Delay Time	t_{pLH}	CLOCK-Q		80		ns
	t_{pHL}			60		
"	t_{pLH} t_{pHL}	CLOCK-$\overline{CARRY}$, $\overline{BORROW}$		60		ns
"	t_{pLH} t_{pHL}	$\overline{LOAD}$-Q		60		ns
"	t_{pLH} t_{pHL}	$\overline{LOAD}$-$\overline{CARRY}$, $\overline{BORROW}$		60		ns
"	t_{pHL}	CLEAR-Q		60		ns
"		CLEAR-$\overline{CARRY}$, $\overline{BORROW}$		60		ns
Data Hold Time	t_{hold}			10		ns
Min. Clock Pulse Width	$t_{w(CK)}$			40		ns
Min. Preset Pulse Width	$t_{w(\overline{LOAD})}$			30		ns
Min. Clear Pulse Width	$t_{w(CL)}$			30		ns
Max. Clock Rise Time	t_r				1	μs
Max. Clock Fall Time	t_f				1	μs
Max.Clock Frequency	f_{MAX}		5	10		MHz
Input Capacitance	C_{IN}		-	5	-	pF

SWITCHING TIME TEST CIRCUIT AND WAVEFORM

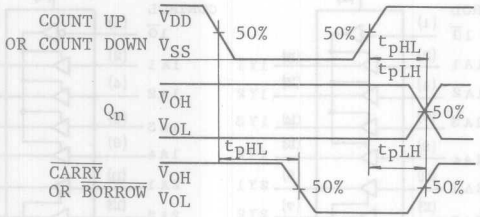
Test Circuit



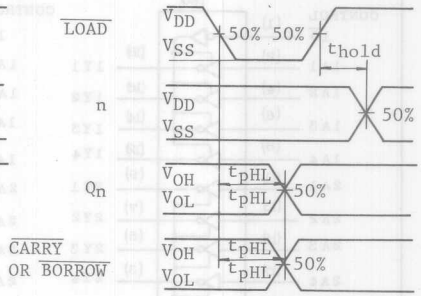
TABLE

TEST NO.	CLEAR	$\overline{LOAD}$	COUNT UP	COUNT DOWN	DATA n
1	L	H	P_{G1}	H	L
1	L	H	H	P_{G1}	L
2	L	P_{G1}	L	L	P_{G2}
3	P_{G1}	P_{G2}	L	L	H

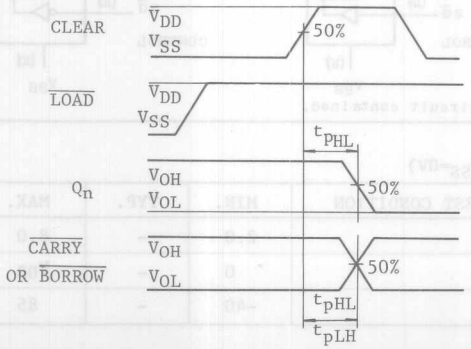
Waveform 1
TEST NO.1



Waveform 2
TEST NO.2



Waveform 3
TEST NO. 3



"C²MOS" DIGITAL INTEGRATED CIRCUIT

TC40H240P TC40H241P TC40H244P

SILICON MONOLITHIC

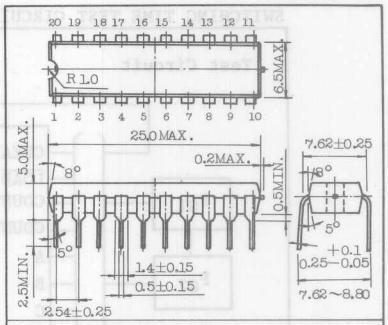
OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

TC40H240P INVERTED 3-STATE OUTPUTS

TC40H241P NONINVERTED 3-STATE OUTPUTS

TC40H244P NONINVERTED 3-STATE OUTPUTS

Unit in mm

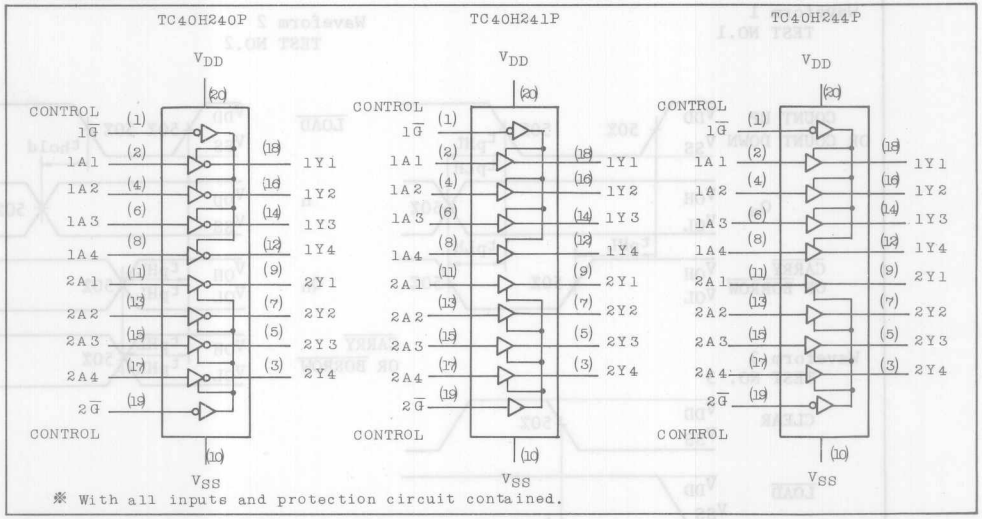


JEDEC	—
TOSHIBA	5 — 25A

MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{SS}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature/Time	T_{sol}	260°C · 10sec	

PIN CONNECTION



※ With all inputs and protection circuit contained.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

TRUTH TABLE

TC40H240P

INPUTS			OUTPUTS
CONTROL		DATA	
$1\overline{G}$	$2\overline{G}$	An	Yn
L	L	L	H
L	L	H	L
H	L	X	1Y1~1Y4 Hz
L	H	X	2Y1~2Y4 Hz
H	H	X	1Y1~1Y4, 2Y1~2Y4 Hz

TC40H241P

INPUTS			OUTPUTS
CONTROL		DATA	
$1\overline{G}$	$2\overline{G}$	An	Yn
L	H	L	L
L	H	H	H
H	H	X	1Y1~1Y4 Hz
L	L	X	2Y1~2Y4 Hz
H	L	X	1Y1~1Y4, 2Y1~2Y4 Hz

TC40H244P

INPUTS			OUTPUTS
CONTROL		DATA	
$1\overline{G}$	$2\overline{G}$	An	Yn
L	L	L	L
L	L	H	H
H	L	X	1Y1~1Y4 Hz
L	H	X	2Y1~2Y4 Hz
H	H	X	1Y1~1Y4, 2Y1~2Y4 Hz

X = Don't care. Hz = High Impedance.

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\lvert I_{OUT}\rvert$<1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\lvert I_{OUT}\rvert$<1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current		I_{OH}	V_{OUT}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.95	-	-0.88	-	-	-0.8	-	mA
Low Level Output Current		I_{OL}	V_{OUT}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	4.7	-	4.4	-	-	4.0	-	mA
Input Voltage	"H" Level	V_{IH}	$\lvert I_{OUT}\rvert$<1μA V_{OUT}=0.5V V_{OUT}=4.5V	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level	V_{IL}		5	-	1.0	-	-	1.0	-	1.0	V
Input Current	"H" Level	I_{IH}	V_{IN}=5.0V	5	-	0.3	-	10^{-5}	3.0	-	1.0	μA
	"L" Level	I_{IL}	V_{IN}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Disable Output Time	"H" Level	I_{DH}	V_{DH}=5.0V	5	-	0.5	-	10^{-4}	0.5	-	30	μA
	"L" Level	I_{DL}	V_{DL}=0.0V	5	-	-0.5	-	-10^{-4}	-0.5	-	-30	μA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	5.0	-	0.005	5.0	-	30	UA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=50pF)

ITEM		SYMBOL	TEST CONDITION	TC40H240P			TC40H241P			TC40H244P			UNIT
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Rise Time		t_{or}	Fig. 1		17	40							ns
Output Fall Time		t_{of}	Fig. 1		17	40							ns
Propagation Delay Time	High Level	t_{pLH}	Fig. 1		24	34							ns
	Low Level	t_{pHL}	Fig. 1		28	38							ns
Disable Output Time	High Level	t_{pHZ}	Fig. 3		27	35							ns
	Low Level	t_{pLZ}	Fig. 3		27	35							ns
Disable Output Time	High Level	t_{pZH}	Fig. 3		24	35							ns
	Low Level	t_{pZL}	Fig. 2		30	42							ns
Input Capacitance		C_{IN}		-	5	-							pF

SWITCHING TIME TEST CIRCUITS AND WAVEFORM

TC40H240P

Fig.1

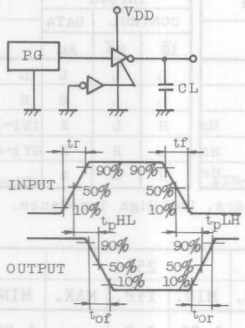


Fig.2

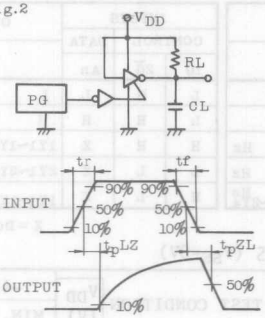
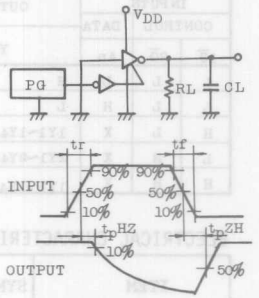


Fig.3



TC40H241P

Fig.1

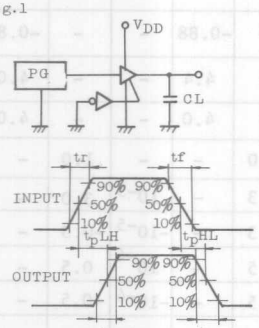


Fig.2

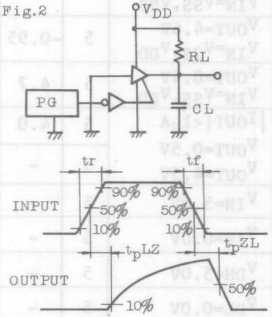
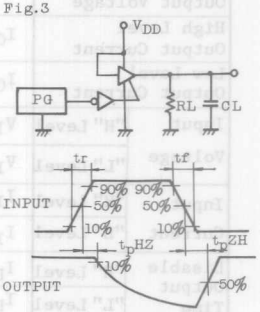


Fig.3



TC40H244P

Fig.1

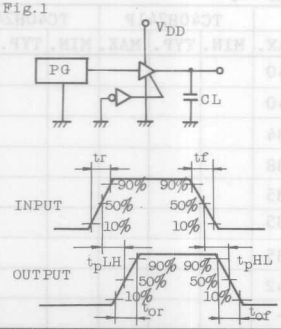


Fig.2

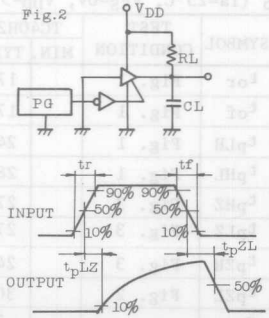
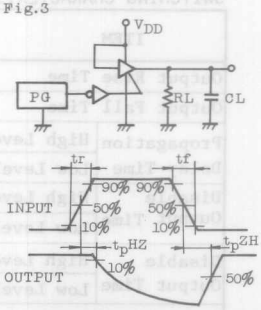


Fig.3



Toshiba **INTEGRATED CIRCUIT**

TECHNICAL DATA

"C²MOS" DIGITAL INTEGRATED CIRCUIT

TC40H242P TC40H243P

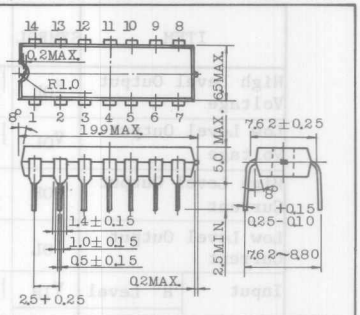
SILICON MONOLITHIC

QUAD BUS TRANSCEIVERS

TC40H242P INVERTED 3-STATE OUTPUTS

TC40H243P NONINVERTED 3-STATE OUTPUTS

Unit in mm



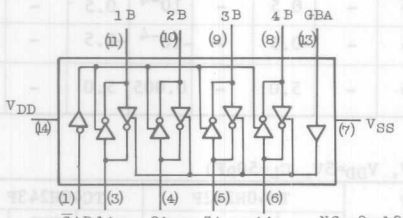
JEDEC	-
TOSHIBA	5-22E

MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature/Time		260°C · 10sec	

PIN CONNECTION & TRUTH TABLE

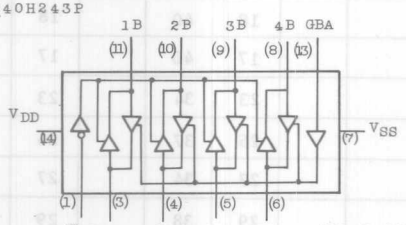
TC40H242P



TC40H242P TRUTH TABLE

CONTROL INPUTS		DATA PORT STATUS				
$\overline{G}AB$	GBA	A		B		
L	L	INPUT	L	OUTPUT	H	
			H		L	
H	H	OUTPUT	L	INPUT	H	
			H		L	
L	H	Don't use				
		High Impedance				

TC40H243P



TC40H243P TRUTH TABLE

CONTROL INPUTS		DATA PORT STATUS				
$\overline{G}AB$	GBA	A		B		
L	L	INPUT	L	OUTPUT	L	
			H		H	
H	H	OUTPUT	L	INPUT	L	
			H		H	
L	H	Don't Vse				
H	L	High Impedance				

※ With all inputs and protection circuit contained.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	
High Level Output Current		I_{OH}	V_{OUT}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.95	-	-0.88	-	-	-0.8	-	mA
Low Level Output Current		I_{OL}	V_{OUT}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	4.7	-	4.4	-	-	4.0	-	
Input Voltage	"H" Level	V_{IH}	$\|I_{OUT}\|<1\mu A$ V_{OUT}=0.5V V_{OUT}=4.5V	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level	V_{IL}		5	-	1.0	-	-	1.0	-	1.0	
Input Current	"H" Level	I_{IH}	V_{IN}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IN}	V_{IN}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Disable Output Time	"H" Level	I_{DH}	V_{DH}=5.0V	5	-	0.5	-	10^{-4}	0.5	-	30	μA
	"L" Level	I_{DL}	V_{DL}=0.0V	5	-	-0.5	-	-10^{-4}	-0.5	-	-30	
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	5.0	-	0.005	5.0	-	30	UA

* All valid input combinations.

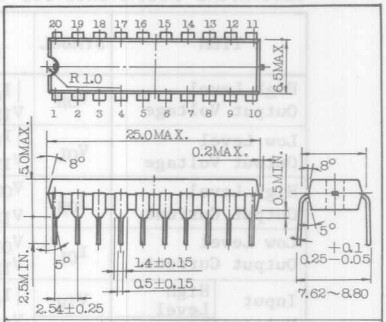
SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=50pF)

ITEM		SYMBOL	TEST CONDITION	TC40H242P			TC40H243P			UNIT
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Rise Time		t_{or}			18	40		18	40	ns
Output Fall Time		t_{of}			17	40		17	40	
Propagation Delay Time	Low to High Level	t_{pLH}			23	34		23	34	ns
	High to Low Level	t_{pHL}			26	37		26	37	
Disable Output Time	"H" Level	t_{pHZ}			27	34		27	34	ns
	"L" Level	t_{pLZ}			29	38		29	38	
Disable Output Time	"H" Level	t_{pZH}			26	38		26	38	ns
	"L" Level	t_{pZL}			32	44		32	44	

"C²MOS" DIGITAL INTEGRATED CIR CUIT
TC40H245P
SILICON MONOLITHIC

TC40H245P OCTAL BUS TRANSCEIVERS

Unit in mm

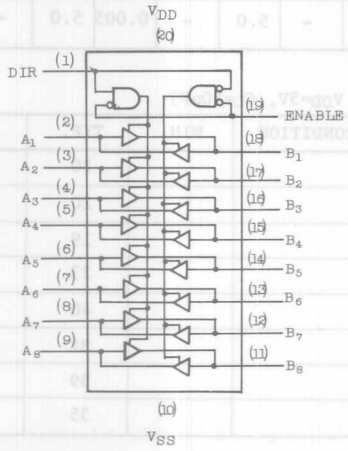


JEDEC	—
TOSHIBA	5 — 25A

MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{SS}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature/Time	T_{sol}	260°C · 10sec	

PIN CONNECTION



CONTROL INPUTS		DATA PORT STATUS
ENABLE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	High Impedance

X = Don't care

- o TC40H245P is a bidirectional bus transceiver with eight circuits that has 3-state outputs.
- o Most suitable for control of 8-bit data line.
- o Its output current is so large that ISTTL can be directly driven by ten inputs.

※ With all inputs and protection circuit contained.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}$, V_{DD}	5	-	0.05	-	0.0	0.05	-	0.05	
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.95	-	-0.88	-	-	-0.8	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	4.7	-	4.4	-	-	4.0	-	
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\| < 1\mu A$ V_{OH}=4.5V V_{OL}=0.5V	5	4.0	-	4.0	-	-	4.0	-	V
	Low Level	V_{IL}		5	-	1.0	-	-	1.0	-	1.0	
Input Current	High Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	µA
	Low Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	5.0	-	0.005	5.0	-	30	µA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=50pF)

ITEM		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}			20	40	ns
Output Fall Time		t_{of}			20	40	
Propagation Delay Time	"H" to "L" Level	tpLH			19	26	ns
	"L" to "H" Level	tpHL			23	29	
Output Disable Time	High Level	tpHZ			40	47	ns
	Low Level	tpLZ			31	38	
Output Disable Time	High Level	tpZH			39	49	ns
	Low Level	tpZL			35	43	

"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H273P
SILICON MONOLITHIC

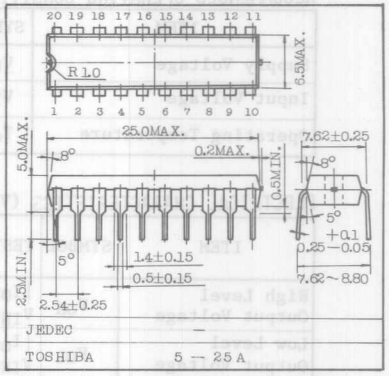
TC40H273P OCTAL "D" TYPE FLIP-FLOPS

TC40H273P is a "D" type flip-flop with eight circuits that has common CLOCK and CLEAR terminals.

CLEAR input is "L" active. In this case, all the outputs come to "L" level regardless of other inputs. When CLEAR input is at "H" level, the DATA is transmitted to the output as it is, by the edge of CLOCK.

The functions and pin assignments of TC40H273P are the same as those of 74LS273.

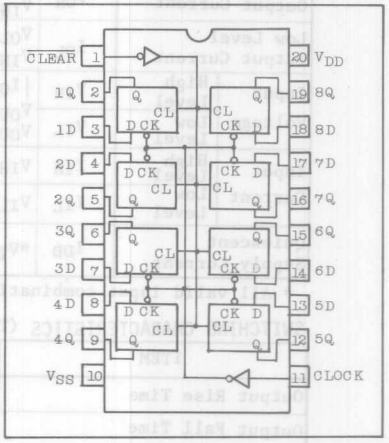
Unit in mm



MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature/Time	T_{sol}	260°C · 10sec	

PIN CONNECTION

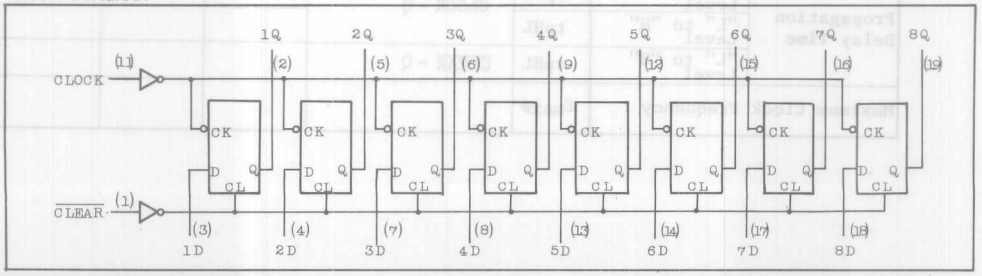


TRUTH TABLE

INPUTS			OUTPUT
$\overline{CLEAR}$	CLOCK	DATA	Q
L	※	※	L
H	↑	H	H
H	↑	L	L
H	L	※	Qo

※ = Don't Care

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MAX.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05		0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	0.44	-	-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1	-	-	0.8	-	mA
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\| < 1\mu A$ V_{OUT}=0.5V V_{OUT}=4.5V	5	4.0	-	4.0	-	-	4.0	-	V
	Low Level	V_{IL}		5	-	1.0	-	-	1.0	-	1.0	V
Input Current	High Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	µA
	Low Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	µA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	µA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V C_L=15pF)

ITEM		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}					ns
Output Fall Time		t_{of}					ns
Propagation Delay Time	"H" to "L" Level	tpLH	CLOCK - Q				ns
	"L" to "H" Level	tpHL					
	"L" to "H" Level	tpHL	$\overline{CLEAR}$ - Q				ns
Maximum Clock Frequency		$f_{max\phi}$					MHz

Toshiba **INTEGRATED CIRCUIT**

TECHNICAL DATA

"C^2MOS" DIGITAL INTEGRATED CIRCUIT

TC40H365P TC40H366P

SILICON MONOLITHIC

HEX BUS DRIVERS

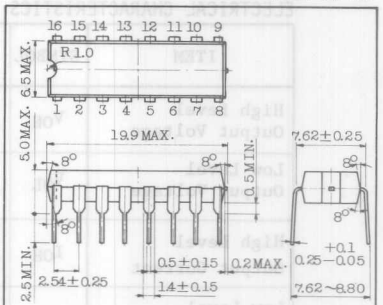
TC40H365P MONINVERTED 3-STATE OUTPUTS
TC40H366P INVERTED 3-STATE OUTPUTS

TC40H365P/TC40H366P is a bus buffer with six circuits that has 3-state outputs.

The outputs become high impedance by setting ENABLE input G_1 or G_2 at "H" level.

Also the output current is so large that ten LSTTL inputs may be directly driven.

Unit in mm



JEDEC	—
TOSHIBA	5-22E

MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5~V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{SS}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5~V_{SS}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature/Time	T_{sol}	260°C · 10sec	

TRUTH TABLE

INPUTS			OUTPUTS
ENABLE $\overline{G_1}$	ENABLE $\overline{G_2}$	DATA A_n	Y_n
L	L	L	L
L	L	H	H
H	*	*	High Impedance
*	H	*	High Impedance

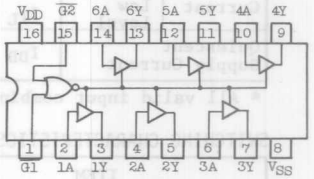
TRUTH TABLE

INPUTS			OUTPUTS
ENABLE $\overline{G_1}$	ENABLE $\overline{G_2}$	DATA A_n	Y_n
L	L	L	H
L	L	H	L
H	*	*	High Impedance
*	H	*	High Impedance

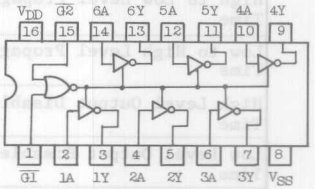
*=Don't care

PIN CONNECTION

TC40H365P



TC40H366P



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.95	-	-0.88	-	-	-0.8	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V V_{IN}=VSS,VDD	5	4.7	-	4.4	-	-	4.0	-	
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\| < 1\mu A$ V_{OH}=4.5V V_{OL}=0.5V	5	4.0	-	4.0	-	-	4.0	-	V
	Low Level	V_{IL}		5	-	1.0	-	-	1.0	-	1.0	
Input Current	High Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	Low Level	I_{IL}	V_{IL}=5.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	1.0	
Quiescent Supply Current		I_{DD}	*V_{IN}=SS,VDD	5	-	5.0	-	0.005	5.0	-	30	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=50pF)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time	tor			17	28	ns
Output Fall Time	tof			15	26	
High to Low Level Propagation Time	tpLH			21	28	ns
Low to High Level Propagation Time	tpHL			26	35	
High Level Output Disable Time	tpHZ			40	46	ns
Low Level Output Disable Time	tpLZ			28	35	
High Level Output Disable Time	tpZH			37	46	ns
Low Level Output Disable Time	tpZL			30	39	
Input Capacitance	C_{IN}		-	5	-	pF

"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H367P, TC40H368P
SILICON MONOLITHIC

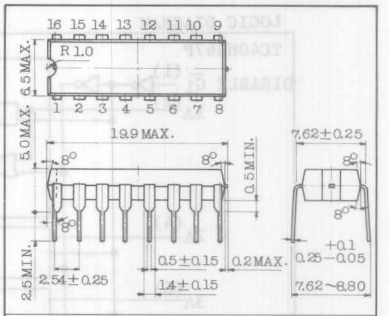
TENTATIVE
TC40H367P 3-STATE NON-INVERTING BUFFERS
TC40H368P 3-STATE INVERTING BUFFERS

TC40H367P and TC40H368P are six-circuit inverting buffers having the 3-state output function respectively. Since the DISABLE inputs for placing the output in the disabled state have the circuit configuration common for two circuits and four circuits, these buffers are suitable for the control of four-bit data line.

The buffers provide large output current capacity, enabling direct drive of 10 LSTTL inputs.

They have the functions and pin connections compatible with TTL 74367 and 74368. And TOSHIBA's original TC5012BP is the same as TC40H367P.

Unit in mm



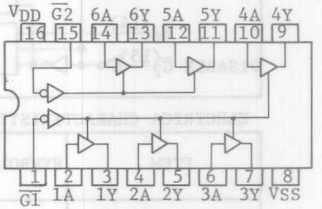
JEDEC	—
TOSHIBA	5-22E

MAXIMUM RATINGS

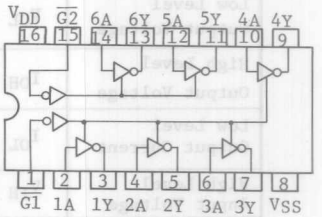
ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 V_{DD}+0.5	V
Input Current	I_{IN}	10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65 150	°C
Lead Temp./Time	T_{sol}	260°C 10 sec	

PIN CONNECTION

TC40H367P



TC40H368P



TRUTH TABLES

TC40H367P

DISABLE INPUT	INPUT	OUTPUT
L	L	L
L	H	H
H	*	Hz

TC40H368P

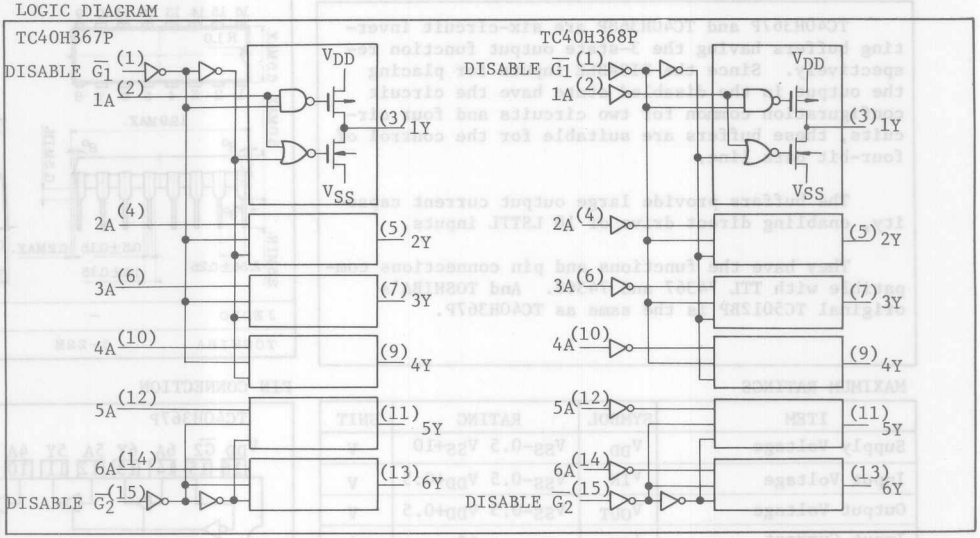
DISABLE INPUT	INPUT	OUTPUT
L	L	H
L	H	L
H	*	Hz

Hz=HIGH IMPEDANCE
* =Don't care

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

LOGIC DIAGRAM



ELECTRICA CHARACTERISTICS (V_{SS} = 0V)

ITEM	SYMBOL	TSET CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|$ <1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05		0.05	
High Level Output Voltage	I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.95	-	-0.88		-	-0.8	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	4.7	-	4.4		-	4.0	-	
High Level Input Voltage	V_{IH}	$\|I_{OUT}\|$ <1μA V_{OH}=4.5V V_{OL}=0.5V	5	4.0	-	4.0		-	4.0	-	V
Low Level Input Voltage	V_{IL}		5	-	1.0	-		1.0	-	1.0	
High Level Input Current	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Low Level Input Current	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current	I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	5.0	-	0.005	5.0	-	30.0	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=50pF, R_L=1kΩ)

ITEM	SYMBOL	TEST CONDITION	TC40H367P			TC40H368P			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Rise Time	t_{or}		-	20	40	-	20	40	ns
Output Fall Time	t_{of}		-	20	40	-	20	40	
(Low→High) Propagation Delay Time	t_{pLH}		-	27	60	-	30	60	ns
(High→Low) Propagation Delay Time	t_{pHL}		-	30	60	-	32	60	
High Level Disable Output Time	t_{pHZ}		-	30	60	-	30	60	ns
Low Level Disable Output Time	t_{pLZ}		-	30	60	-	30	60	
High Level Disable Output Time	t_{pZH}		-	27	60	-	27	60	ns
Low Level Disable Output Time	t_{pZL}		-	30	60	-	30	60	
Input Capacity	C_{IN}		-	5	-	-	5	-	pF
Disable Output Capacity	Cout		-	20	-	-	20	-	pF

"C²MOS" DIGITAL INTEGRATED CIRCUIT

TC40H373P

SILICON MONOLITHIC

TC40H373P OCTAL "D" TYPE LATCH (3-STATE OUTPUTS)

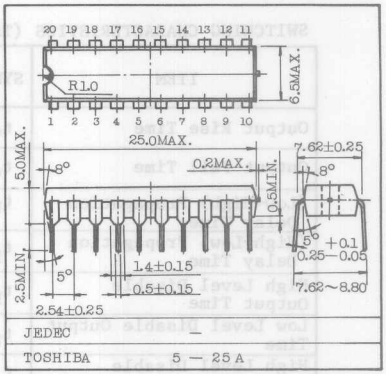
Unit in mm

TC40H373P is a "D" type latch with eight circuits that 3-state output control terminals.

When OUTPUT-CONTROL input is at "H" level, if ENABLE is set at "H" level, the data is output as it is or if ENABLE is set at "L" level, the output holds the data immediately before ENABLE is changed from "H" to "L".

Regardless of other inputs, the output becomes high impedance by setting OUTPUT-CONTROL at "H" level.

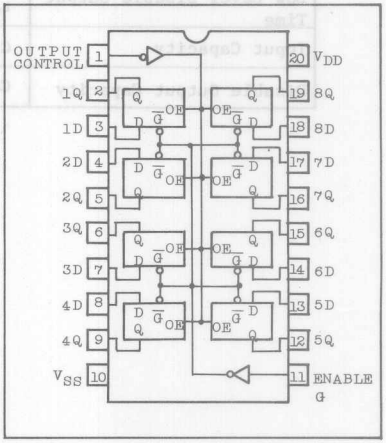
The eight circuits are common to OUTPUT-CONTROL input and ENABLE input. The functions and pin assignment of TC40H373P are the same as those of 74LS373.



MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature/Time	T_{sol}	260°C · 10sec	

PIN CONNECTION

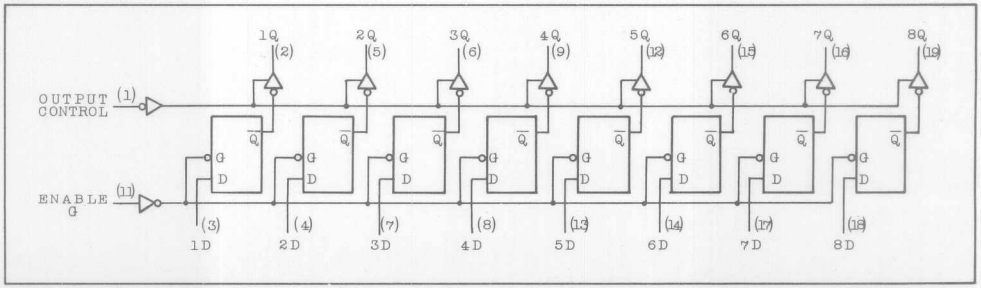


TRUTH TABLE

INPUTS			OUTPUTS
OUTPUT CONTROL	ENABLE G	DATA	Q
L	H	H	H
L	H	L	L
L	L	*	Qo
H	*	*	High Impedance

*=Don't care

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Level		V_{OH}	$\lvert I_{OUT}\rvert$ < 1μA V_{IN}=V_{SS},V_{DD}	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Level		V_{OL}	$\lvert I_{OUT}\rvert$ < 1μA V_{IN}=V_{DD},V_{SS}	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V V_{IN}=V_{SS},V_{DD}	5	-0.95	-	-0.88	-	-	-0.8	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V V_{IN}=V_{DD},V_{SS}	5	4.7	-	4.4	-	-	4.0	-	mA
Input Voltage	High Level	V_{IH}	$\lvert I_{OUT}\rvert$ < 1μA V_{OUT}=0.5V	5	4.0	-	4.0	-	-	4.0	-	V
	Low Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-	-	1.0	-	1.0	V
Input Current	High Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	Low Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current		I_{DD}	*V_{IN}=V_{SS},V_{DD}	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

*All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=50pF)

ITEM		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}		-	20	35	ns
Output Fall Time		t_{of}		-	20	35	ns
Propagation Delay Time	"H" to "L" Level	tpLH	DATA - Q	-	39	50	ns
	"L" to "H" Level	tpHL		-	33	43	ns
Propagation Delay Time	"H" to "L" Level	tpLH	ENABLE -Q	-	39	50	ns
	"L" to "H" Level	tpHL		-	35	46	ns
Output Disable Time	High Level	tpHZ	OUTPUT CONTROL - Q	-	25	32	ns
	Low Level	tpLZ		-	27	35	ns
Output Disable Time	High Level	tpZH	R_L=1kΩ	-	27	35	ns
	Low Level	tpZL		-	30	39	ns

"C²MOS" DIGITAL INTEGRATED CIRCUIT

TC40H374P

SILICON MONOLITHIC

TC40H374P OCTAL "D" TYPE FLIP-FLOPS

TC40H374P is a "D" type flip-flop with eight circuits that has 3-STATE output control terminals.

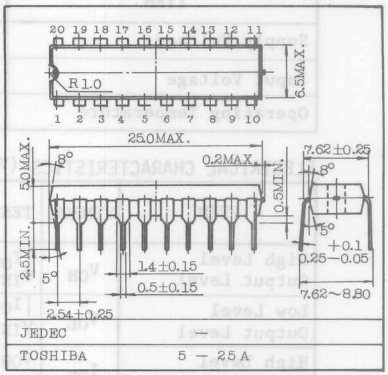
When OUTPUT-CONTROL input is at "L" level, the data is transmitted to the output by the rising edge of CLOCK.

If OUTPUT-CONTROL input is set at "H" level, the output becomes high impedance regardless of other outputs.

CLOCK anc OUTPUT-CONTROL input are common to eight circuits.

The functions and pin assignments of TC40H374P are the same as those of 74LS166.

Unit in mm

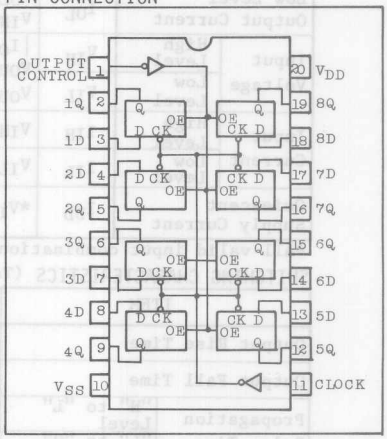


JEDEC	—
TOSHIBA	5 − 25A

MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature/Time	T_{sol}	260°C · 10sec	

PIN CONNECTION

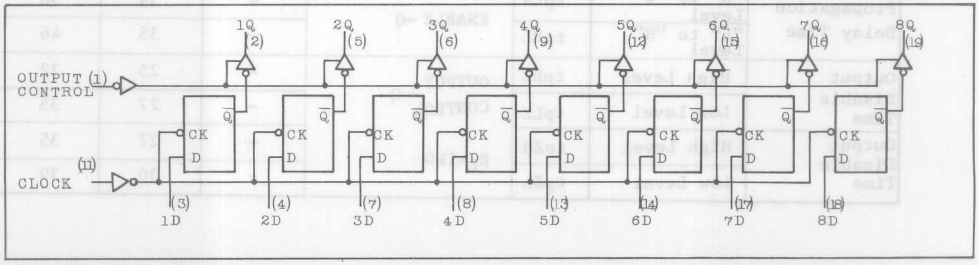


TRUTH TABLE

INPUTS			OUTPUT
OUTPUT CONTROL	CLOCK	DATA	Q_n
L	↑	H	H
L	↑	L	L
L	↓	※	Q_0
H	※	※	High Impedance

※ Don't care

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05		0.05	
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.95	-	-0.88	-	-	-0.8	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	4.7	-	4.4	-	-	4.0	-	
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\| < 1\mu A$ V_{OUT}=0.5V V_{OUT}=4.5V	5	4.0	-	4.0	-	-	4.0	-	V
	Low Level	V_{IL}		5	-	1.0	-	-	1.0	-	1.0	
Input Current	High Level	V_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	Low Level	V_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=50pF)

ITEM		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	CLOCK - Q	-	20	35	ns
Output Fall Time		t_{of}		-	20	35	
Propagation Delay Time	"H" to "L" Level	tpLH		-	39	50	ns
	"L" to "H" Level	tpHL		-	35	46	
Output Disable Current	High Level	tpHZ	OUTPUT CONTROL - Q R_L=1kΩ	-	25	32	ns
	Low Level	tpLZ		-	27	35	
	High Level	tpZH		-	27	35	
	Low Level	tpZL		-	30	39	
Maximum Clock Frequency		$f_{max\phi}$		10	20	-	MHz

"C²MOS" DIGITAL INTEGRATED CIRCUIT

TC40H375P

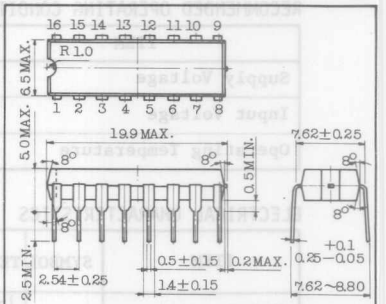
SILICON MONOLITHIC

TC40H375P 4-BIT BISTABLE LATCH

TC40H375P is a latch with four circuits that has ENABLE input common to two circuits.

When ENABLE input is at "H" level, the data input is transmitted to the output as it is. If ENABLE input is changed over from "H" to "L", the output holds the DATA input existing immediately before ENABLE input falls. When ENABLE input is at "L" level, the outputs are not affected by the change in DATA input.

Unit in mm

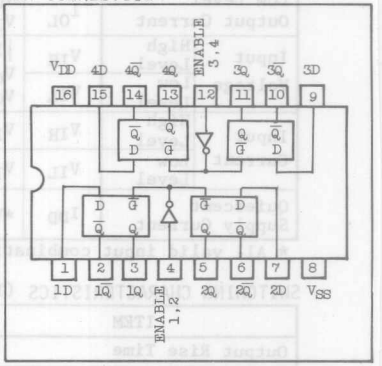


JEDEC	—
TOSHIBA	5—22E

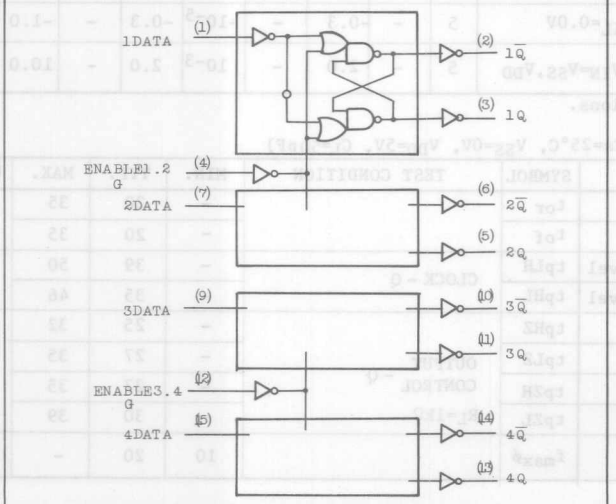
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature/Time	T_{sol}	260°C · 10sec	

PIN CONNECTION



LOGIC DIAGRAM



※ With all inputs and protection circuit contained.

TRUTH TABLE

INPUTS		OUTPUTS	
DATA	ENABLE	Q	Q̄
L	H	L	H
H	H	H	L
X	L	No Change	

X = Don't Care

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	MAX.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.52	-	0.0	0.05		0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	0.44	-	-	-0.36	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1	-	-	0.8	-	mA
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\| < 1\mu A$ V_{OUT}=0.5V	5	4.0	-	4.0	-	-	4.0	-	V
	Low Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-	-	1.0	-	1.0	V
Input Current	High Level	V_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	Low Level	V_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	10	2.0	-	10.0	μA

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=15pF)

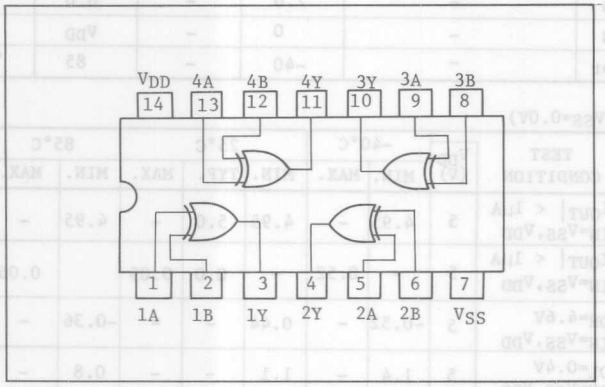
ITEM		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}		-	20	40	ns
Output Fall Time		t_{of}		-	20	40	ns
Propagation Delay Time	"H" to "L" Level	tpLH	DATA - Q, $\overline{Q}$	-	45		ns
	"L" to "H" Level	tpHL		-	38		ns
	"H" to "L" Level	tpLH	ENABLE - Q, $\overline{Q}$	-	43		ns
	"L" to "H" Level	tpHL		-	41		ns
Minimum Enable Pulse Width		tW		-	45		ns
Minimum Hold Time		t_{hold}		-	15		ns
Minimum Hot Up Time		tset-up		-	28		ns
Input Capacitance		C_{IN}		-	5		pF

"C²MOS" DIGITAL INTEGRATED CIRCUIT
TC40H386P
SILICON MONOLITHIC

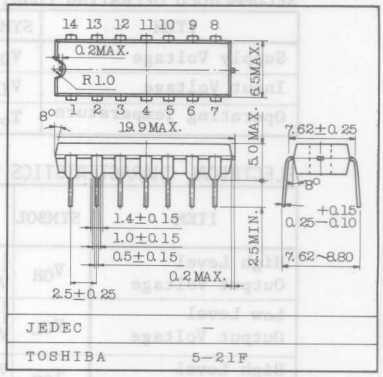
TENTATIVE

TC40H386P QUAD 2-INPUT EXCLUSIVE OR GATES

PIN CONNECTION



Unit in mm



JEDEC	—
TOSHIBA	5-21F

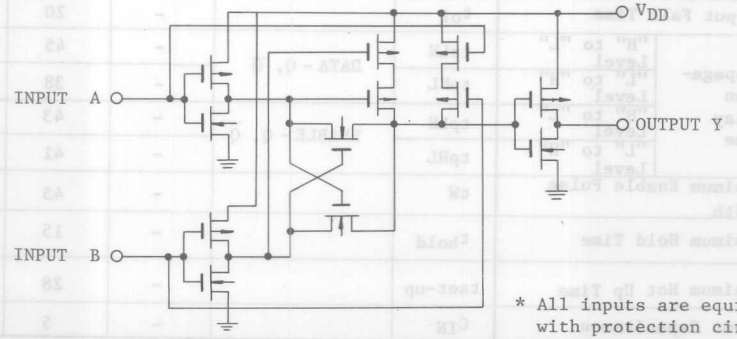
MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{DD}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	V_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temp.	Tstg	-65∿150	°C
Lead Temp./ Time	Tsol	260°C·10 sec	

TRUTH TABLE

INPUTS		OUTPUT
B	A	Y
L	L	L
L	H	H
H	L	H
H	H	L

CIRCUIT DIAGRAM



* All inputs are equipped with protection circuit.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temp.	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|$ <1μA, $V_{IN}=V_{SS}, V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|$ <1μA, $V_{IN}=V_{SS}, V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current	I_{OH}	V_{OH}=4.6V, $V_{IN}=V_{SS}, V_{DD}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V, $V_{IN}=V_{SS}$ V_{DD}	5	1.4	-	1.1		-	0.8	-	mA
High Level Input Voltage	V_{IH}	$\|I_{OUT}\|$ <1μA, V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
Low Level Input Volatge	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-		1.0	-	1.0	V
Input Current "H" Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current	I_{DD}	*$V_{IN}=V_{SS}, V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

ITEM		SYMBOL	TEST CONDITIONS	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig. 1	5	-	17	31	ns
Output Fall Time		t_{of}	Fig. 1	5	-	14	27	ns
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 1	5	-	21	31	ns
	(H-L)	t_{pHL}		5	-	21	31	ns
Propagation Delay Time	(L-H)	t_{pLH}	Fig. 2	5	-	24	24	ns
	(H-L)	t_{pHL}		5	-	26	39	ns
Input Capacitance		C_{IN}			-	5		pF

SWITCHING TIME TEST CIRCUITS

Fig. 1

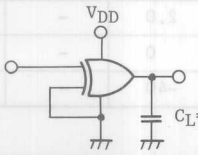
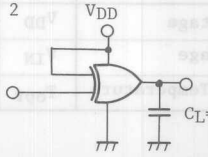


Fig. 2



"C²MOS" DIGITAL INTEGRATED CIRCUIT

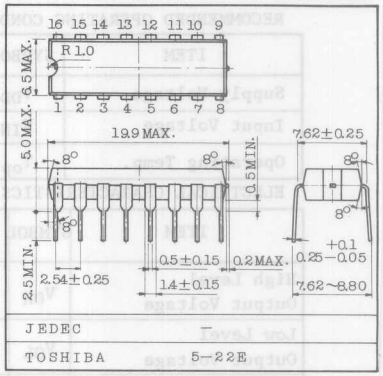
TC50H000P TC50H001P

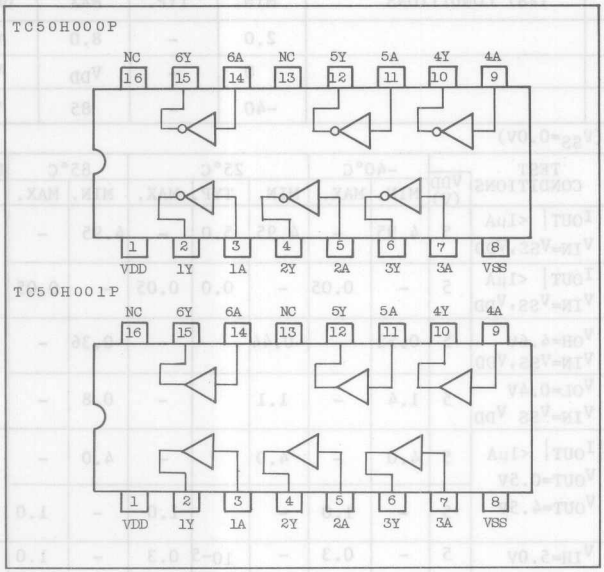
SILICON MONOLITHIC

TC50H000P HEX BUFFER/CONVERTER INVERTING TYPE

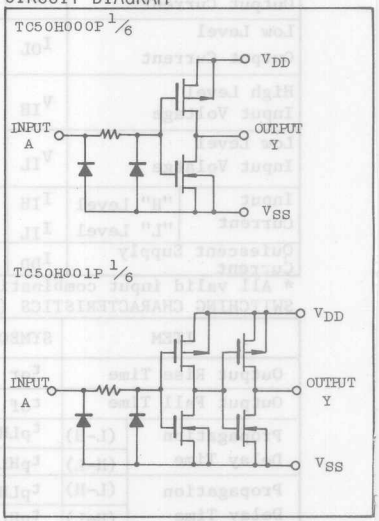
TC50H001P HEX BUFFER/CONVERTER NONINVERTING TYPE

Unit in mm





CIRCUIT DIAGRAM



MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5∿V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5∿V_{SS}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5∿V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature/Time	T_{sol}	260°C · 10sec	

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	-	8.0	V
Input Voltage	V_{IN}		0	-	18	V
Operating Temperature	T_{opr}		-40	-	85	°C

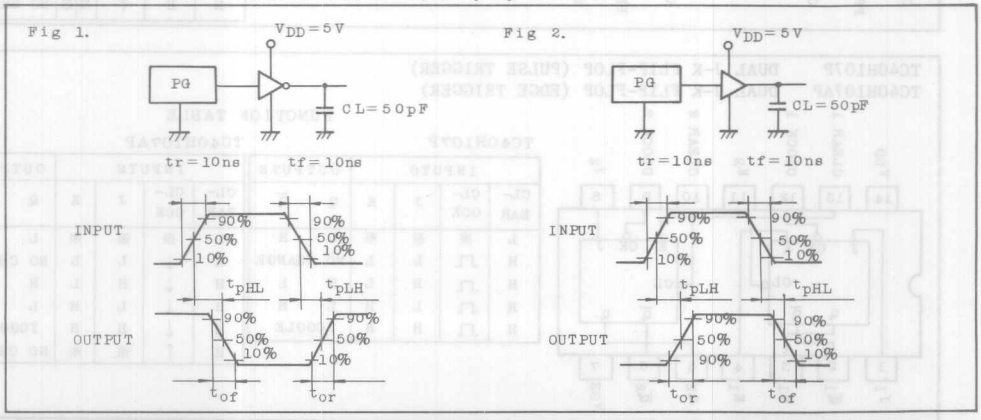
ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

ITEM		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS},V_{SS}$	5	-	0.05	-	0.0	0.05		0.05	
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-1.04	-	-0.88		-	-0.72	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	2.8	-	2.2		-	1.6	-	
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\| < 1\mu A$ V_{OUT}=0.5V V_{OUT}=4.5V	5	4.0	-	4.0		-	4.0	-	V
	Low Level	V_{IL}		5	-	1.0	-		1.0	-	1.0	
Input Current	High Level	I_{IH}	V_{IH}=5.0V	5	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	Low Level	I_{IL}	V_{IL}=0.0V	5	-	-0.3	-	-10^{-5}	-0.3	-	1.0	
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	1.0	μA

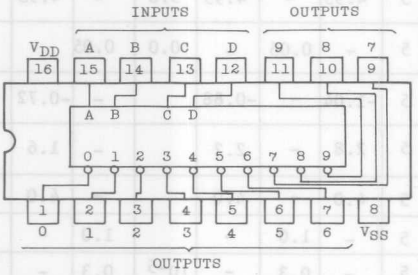
SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, CL=50PF)

ITEM		SYMBOL	TEST CONDITION	TC50H000P			TC50H001P			UNIT
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Rise Time		t_{or}	Fig. 1, 2	-	20	40	-	20	40	ns
Output Fall Time		t_{of}		-	20	40	-	20	40	
Propagation Delay time	"H" to "L" Level	t_{pLH}	Fig. 1, 2	-	18	36	-	22	44	ns
	"L" to "H" Level	t_{pHL}		-	15	30	-	19	38	

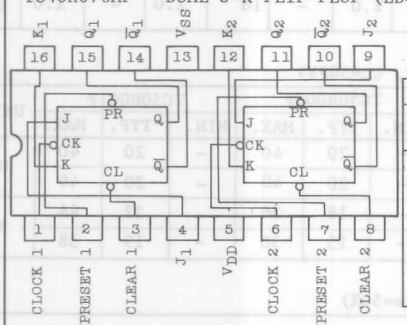
SWITCHING TIME TEST CIRCUITS (f_{IN}=1MHz, Duty Cycle=50%)



TC40H042P BCD-TO-DECIMAL DECODER/DRIVER



TC40H076P DUAL J-K FLIP-FLOP (PULSE TRIGGER)
TC40H076AP DUAL J-K FLIP-FLOP (EDGE TRIGGER)



FUNCTION TABLE

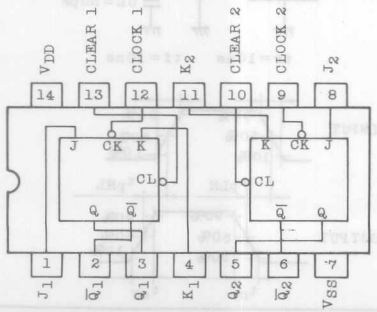
TC40H076P

INPUTS					OUTPUTS	
PRE-SET	CL-EAR	CL-OCK	J	K	Q	$\overline{Q}$
L	H	※	※	※	H	L
H	L	※	※	※	L	H
L	L	※	※	※	H	H
H	H	⎍	L	L	NO CHANGE	
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

TC40H076AP

INPUTS					OUTPUTS	
PRE-SET	CL-EAR	CL-OCK	J	K	Q	$\overline{Q}$
L	H	※	※	※	H	L
H	L	※	※	※	L	H
L	L	※	※	※	H	H
H	H	↓	L	L	NO CHANGE	
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	↑	※	※	NO CHANGE	

TC40H107P DUAL J-K FLIP-FLOP (PULSE TRIGGER)
TC40H107AP DUAL J-K FLIP-FLOP (EDGE TRIGGER)



FUNCTION TABLE

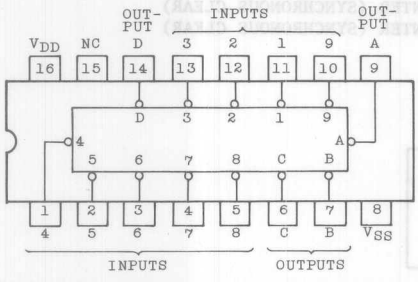
TC40H107P

INPUTS				OUTPUTS	
CL-EAR	CL-OCK	J	K	Q	$\overline{Q}$
L	※	※	※	L	H
H	⎍	L	L	NO CHANGE	
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

TC40H107AP

INPUTS				OUTPUTS	
CL-EAR	CL-OCK	J	K	Q	$\overline{Q}$
L	※	※	※	L	H
H	↓	L	L	NO CHANGE	
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	↑	※	※	NO CHANGE	

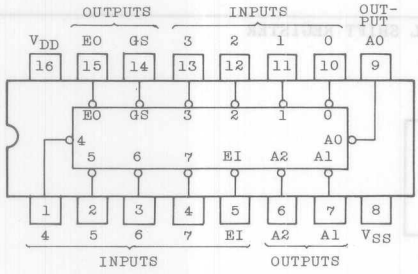
TC40H147P 10 LINE-4 LINE PRIORITY ENCODER



FUNCTION TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	A	B	C	D
L	H	H	H	H	H	H	H	H	L	H	H	H
※	L	H	H	H	H	H	H	H	H	L	H	H
※	※	L	H	H	H	H	H	H	L	L	H	H
※	※	※	L	H	H	H	H	H	H	H	L	H
※	※	※	※	L	H	H	H	H	L	H	L	H
※	※	※	※	※	L	H	H	H	H	L	L	H
※	※	※	※	※	※	L	H	H	L	L	L	H
※	※	※	※	※	※	※	L	H	H	H	H	L
※	※	※	※	※	※	※	※	L	L	H	H	L
H	H	H	H	H	H	H	H	H	H	H	H	H

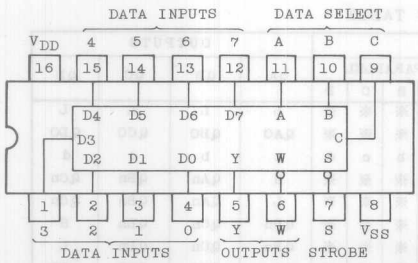
TC40H148P 8 LINE-TO-3 PRIORITY ENCODER



FUNCTION TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A0	A1	A2	GS	EO
L	L	H	H	H	H	H	H	H	H	H	H	L	H
L	※	L	H	H	H	H	H	H	L	H	H	L	H
L	※	※	L	H	H	H	H	H	H	L	H	L	H
L	※	※	※	L	H	H	H	H	L	L	H	L	H
L	※	※	※	※	L	H	H	H	H	H	L	L	H
L	※	※	※	※	※	L	H	H	L	H	L	L	H
L	※	※	※	※	※	※	L	H	H	L	L	L	H
L	※	※	※	※	※	※	※	L	L	L	L	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
H	※	※	※	※	※	※	※	※	H	H	H	H	H

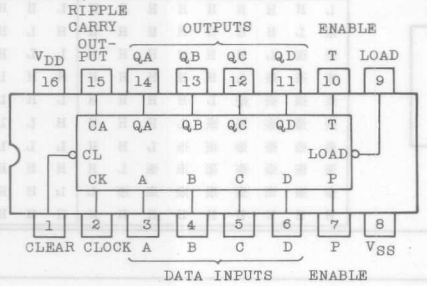
TC40H151P 1-OF-8 DATA SELECTOR/MULTIPLEXER



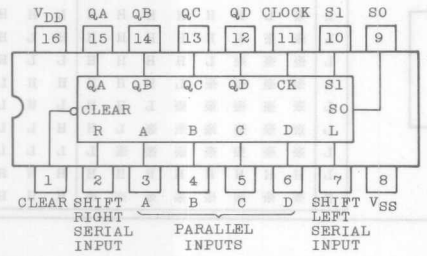
FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
A	B	C	S	Y	W
※	※	※	H	L	H
L	L	L	L	D0	D0
H	L	L	L	D1	D1
L	H	L	L	D2	D2
H	H	L	L	D3	D3
L	L	H	L	D4	D4
H	L	H	L	D5	D5
L	H	H	L	D6	D6
H	H	H	L	D7	D7

TC40H160P SYNCHRONOUS 4-BIT DECADE COUNTER (ASYNCHRONOUS CLEAR)
TC40H161P SYNCHRONOUS 4-BIT BINARY COUNTER (ASYNCHRONOUS CLEAR)
TC40H162P SYNCHRONOUS 4-BIT DECADE COUNTER (SYNCHRONOUS CLEAR)
TC40H163P SYNCHRONOUS 4-BIT BINARY COUNTER (SYNCHRONOUS CLEAR)



TC40H194P 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER



FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	※	※	※	※	※	※	※	※	※	L	L	L	L
H	※	※	L	※	※	※	※	※	※	QA0	QB0	QC0	QD0
H	H	H	↑	※	※	a	b	c	d	a	b	c	d
H	L	H	↑	※	H	※	※	※	※	H	QAn	QBn	QCn
H	L	H	↑	※	L	※	※	※	※	L	QAn	QBn	QCn
H	H	L	↑	H	※	※	※	※	※	QBn	QCn	QDn	H
H	H	L	↑	L	※	※	※	※	※	QBn	QCn	QDn	L
H	L	L	※	※	※	※	※	※	※	QA0	QB0	QC0	QD0